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Final Technical Report
October 1989

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COMPUTER-AIDED DESIGN FOR BUILT-IN-TEST (CADBIT) - BIT Library

Grumman Aerospace Corporation

Hank Baluta

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The Computer Aided Design for Built-In-Test (CADBIT) Final Report consists of three volumes organized as follows. Volume I is a general description including introduction, automated procedure, data base, menus, CAD and BIT survey, and recommendations. Volume II contains a description of the BIT data base library element and BIT library elements for 13 BIT techniques, which were found to be suitable for CADBIT. Volume III contains the CADBIT software requirements specification to be used as a basis for encoding the CADBIT software modules and the creation of its data base.

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1.0 SUMMARY

This report is one of three volumes. The Executive Summary decribes the entire CAD-BIT effort and the following Volume Summary is a description of this volume.

1.1 EXECUTIVE SUMMARY

CAD-BIT is a development program to specify the implementation of an automated procedure to integrate Built-In-Test (BIT) into the design of Printed Circuit Boards (PCBs) on Computer-Aided Design (CAD) workstations. When fully developed, the CAD-BIT software will be capable of operating on generic workstations meeting various standards. These standards include those for operating system (UNIX), programming language (C), and graphical data interchange Initial Graphics Exchange Specification (IGES).

The purpose of this program was to develop the design of the automated procedure, the associated BIT data base, and a software specification for the CAD-BIT module ready for encoding. No coding of the CAD-BIT Module (CBM) was performed except as necessary to test and verify feasibility. CAD workstations and BIT techniques and their applications were also surveyed to determine standards required for the CAD-BIT module implementation and to establish requirements for and define the structure of the BIT data base.

1.1.1 SCOPE

This report describes the development of the CAD-BIT automated procedure, the associated Data Base of BIT Functions, and software specification developed during this contract. The contents of this report are organized into the three volumes described below.

Volume I Technical Issues

Volume I is a general CAD-BIT description and provides useful information for any type of involvement with CAD-BIT. It begins with an Executive Summary describing the work performed under the CAD-BIT contract. It is followed by a detailed description of the automated procedure. The description contains text, flow diagrams of the procedure operations and its data, sets of menu sequences showing menu options, selections, and resulting operations. Algorithms and formulas are included. The CAD-BIT Data Base and its files are described.

Additional topics in Volume I include Menus, the CAD-BIT Feasibility Demonstration, BIT and CAD workstation surveys and Standards Recommendations, SMART-BIT Applications, and a Automated Procedure Evaluation. The Volume also includes an appendix with a BIT library example for the On-Board ROM BIT Technique.

Volume II BIT Library

Volume II contains a description of the BIT data base library elements and BIT library elements for the thirteen BIT techniques listed below. The data in Volume II will be used to encode CAD-BIT's BIT technique data base during the implementation phase. In addition, it illustrates the required data for adding new BIT techniques. It also provides useful data to the future circuit designer / CAD-BIT user on the BIT techniques, their implementation, and the default circuit components.

- On-Board ROM
- Microprocessor BIT
- Microdiagnostics
- On-Board Integration of VLSI Chips BIT (OBIVCB)
- Built-In Logic Block Observer (BILBO)
- Error Detection and Correction Codes
- Scan
- Digital Wraparound
- Pseudo Random Pattern Generator with Multiple Input Shift Register (PRPG/MISR)
- Comparator
- Voltage Summing
- Redundancy
- Analog Wraparound

Volume III CAD-BIT Software Specification

Volume III contains the CAD-BIT Software Requirements Specification (SRS). This SRS establishes the requirements for the Computer Software Configuration Item (CSCI) identified as Computer-Aided Design for Built-In-Test (CAD-BIT) System. It will be used during the implementation as the basis for encoding the CAD-BIT software modules and the creation of its data base.

1.1.2 PURPOSE

The purpose of the CAD-BIT system is to provide an automated procedure to aid the electronic circuit designer in the selection of BIT techniques, the insertion of the associated BIT circuitry into the PCB design, and to provide a post design evaluation of the penalties incurred by the addition of BIT circuitry into the PCB functional design.

1.2 VOLUME II SUMMARY

The organization of Volume II of the CAD-BIT Final Report is shown in Figure 1-1. The bulk of the volume is a set of data packages for a variety of BIT techniques. The packages are labeled in Figure 1-1 as "Library Element for Techniques n".

Preceding the data packages is the Data Base of BIT Functions Introduction. The introduction describes the criteria used in selecting the BIT techniques for inclusion in the BIT library, along with the list of the techniques and a short summary of each. A description of the data elements for each technique is also provided.

2.0 DATA SOURCES

One of the sources of data for the library was a BIT survey, an investigation and analysis of design of PCBs from a variety of electronic equipment systems including analog, digital and hybrid PCBs. The details of the survey are described in Volume I of the CAD-BIT final report.

In order to obtain a greater scope and more detailed information on the various BIT techniques, a literature search was also conducted and over 100 papers on BIT were accumulated and reviewed. Papers especially pertinent to the enclosed techniques are listed in the Bibliography contained at the end of each technique library element.

3.0 CRITERIA FOR BIT TECHNIQUE SELECTION

Certain criteria concerning the selection of BIT techniques for the library were arrived at as a result of contractor queries at the beginning of the study. These criteria govern various aspects of the definition of the BIT Library and are as follows:

- Self Contained

  The BIT technique shall be self contained within the Line Replaceable Module (LRM) or Printed Circuit Board (PCB). All of the hardware and software necessary to conduct the Built-In-Test shall be resident on the LRM itself with the exception of BIT Initiate and Pass/Fail signals.
- In Flight/Flight Line Maintenance

  The techniques to be considered are primarily for In Flight or Flight Line Maintenance (as opposed to intermediate level or depot maintenance).

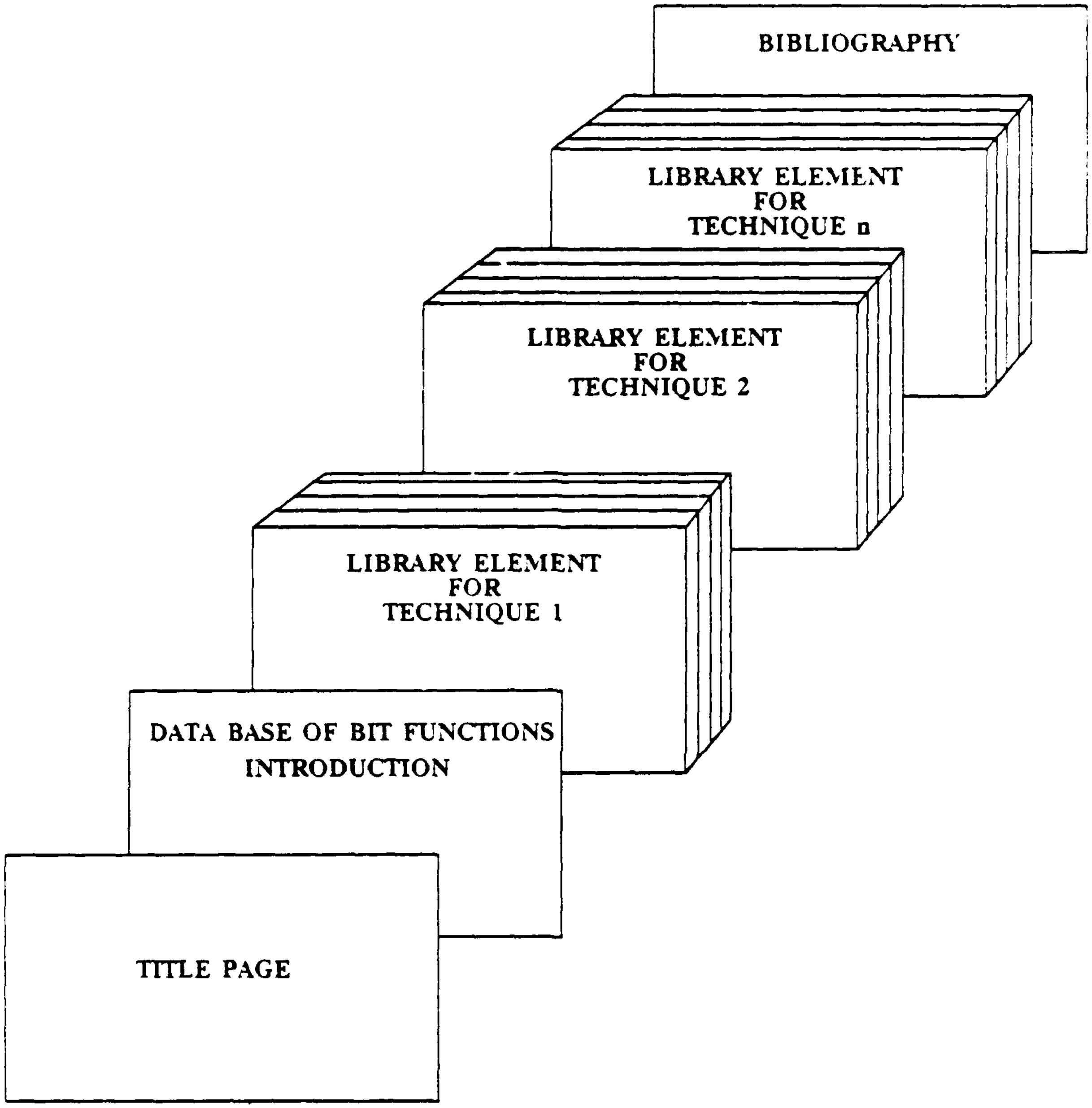


FIGURE 1-1
ORGANIZATION OF VOLUME II OF CAD-BIT FINAL REPORT

- Fault Detection

  The techniques are for fault detection. If a technique provides fault isolation, it will not be considered an advantage if there is a real estate or power penalty associated with the fault isolation capability.

- Modifiable

  The structure of the data base shall be such that modifications can be made as knowledge or data in the technique is accumulated.

- Open Ended

  The data base shall be open ended to allow inclusion of additional BIT techniques as they are developed.

- LRM Design only

  Some CAD systems support the design of semi-custom integrated circuits concurrently with the design of the LRM on which the integrated circuits will reside. CAD-BIT will only facilitate inclusion of BIT into the LRM. CAD-BIT may utilize BIT in the integrated circuit, but is not intended as a vehicle to incorporate BIT into the integrated circuit. However, the system can be easily expanded to do so.

4.0 DESCRIPTION OF CAD-BIT LIBRARY CONTENT

4.1 LIST OF BIT TECHNIQUES

As a result of the BIT survey, a representative list of BIT techniques was selected for the Library Package. The list is wide ranging and represents a broad cross section of circuit design applications. Besides addressing the three general classifications of digital, analog and hybrid, the list also includes BIT techniques applicable to LRM's that contain microprocessors, microprogrammed machines and Very High Speed Integrated Circuits (VHSIC). Additional techniques allow the designer to insert Built-In-Test Equipment on the interior of his design or be strictly external to his original design. A list of BIT techniques supplied in this Volume is shown below with a brief summary of each technique

DIGITAL

On-Board ROM
Microprocessor BIT
Microdiagnostics

On Board Integration of VLSI Chips Bit (OBIVCB)
Built-In Logic Block Observer (BILBO)
Error Detection and Correction Codes
Scan
Digital Wraparound
Pseudo Random Pattern Generator/Multiple Input Shift Register (PRPG/MISR)

ANALOG

Comparator
Voltage Summing
Redundancy

HYBRID

Analog Wraparound

4.1.1 ON-BOARD ROM

BIT test patterns and good machine responses are stored in on-board ROM. As each test pattern is applied the output of the Circuit Under Test (CUT) is compared to the known good machine responses. A mismatch indicates an LRM failure.

4.1.2 MICROPROCESSOR BIT

The inherent intelligence of the microprocessor is used to test itself and associated peripheral circuitry such as memory and Input/Output (I/O). A self test program is written to exercise circuitry within and outside of the microprocessor integrated circuit. The BIT program is stored in ROM.

4.1.3 MICRODIAGNOSTICS

Microprogrammed processors have their instruction repertoire defined in external ROM instead of internal logic of conventional processors. Special instructions can be defined which will test both internal and external processor hardware in a very efficient manner. These BIT instructions are added to the normal instructions resident in external ROM.

4.1.4 ON BOARD INTEGRATION OF VLSI CHIPS BIT (OBIVCB)

Many current Very Large Scale Integration (VLSI) chips are designed with an internal BIT or contain hardware such as scan registers to facilitate their own checkout. This technique integrates the chips internal BIT with the overall BIT of the LRM on which these chips are resident.

4.1.5 BUILT IN LOGIC BLOCK OBSERVER (BILBO)

Circuit structures can be configured to function as a variety of BIT devices, such as, a pseudo random pattern generator or a multiple input shift register. This circuit is configured by different binary patterns on two input control lines and the circuit can also serve as a bank of normal CUT flip-flops. Thus, this one design can be placed throughout the CUT and can be configured and reconfigured during test to provide a variety of BIT functions.

4.1.6 ERROR DETECTION AND CORRECTION CODES

Extra bits can be added to digital words containing information on the validity of the data when the word is transmitted or stored in memory. Hardware exists which examine these extra bits and can determine whether any bits have erroneously changed state during the manipulation of the word.

4.1.7 SCAN

The main principle of SCAN is to provide a redundant flip-flop (FF) for each FF in the normal circuitry so that at a predetermined instance, the secondary FF can be set to the state of its corresponding primary one. The secondary FFs are connected as a shift register so that the state of the machine, as captured by the secondary FFs, can then be shifted to the outside of the CUT for analysis for proper operation.

4.1.8 DIGITAL WRAPAROUND

LRMs that contain a microprocessor and some digital input and digital output circuits can have their I/O checked out with the addition of gates that wrap the output to the input. The microprocessor serves as test controller, stimuli generator and response comparator.

4.1.9 PSEUDO RANDOM PATTERN GENERATOR WITH MULTIPLE INPUT SHIFT REGISTER (PRPG/MISR)

This technique combines two BIT circuits to accomplish a checkout of the CUT. A linear feedback shift register is a source of test vectors for input to the CUT. A CUT output signature is accumulated in the Multiple Input Shift Register for the duration of the pseudo random pattern sequence. The signature is then compared to a good machine signature to determine a pass or fail status of the CUT.

4.1.10 COMPARATOR

An analog test signal source located on the LRM is fed into a CUT analog channel. The output of the analog channel is compared to a predetermined reference signal (also generated on the LRM) via a comparator to determine whether the channel is operating properly.

4.1.11 VOLTAGE SUMMING

LRMs that generate a set of simple signals (such as DC Levels or Power Supply Voltages) can be tested by combining their signals into a single sum and then comparing this sum with a known good value of signal also generated on the LRM. An excessive variation of any single signal will be reflected in the sum and will be detected by the comparator to flag a fault condition.

4.1.12 REDUNDANCY

Redundancy requires duplicating the normal CUT and stimulating both the CUT and the redundant CUT from the same signal source and comparing the outputs with a comparator. If the comparator detects a difference between the outputs it sets an error flag.

4.1.13 ANALOG WRAPAROUND

LRMs containing a microprocessor and analog input and output can have their I/O checked out with the addition of analog switches that wrap the output around to the LRMs. The LRMs contain a microprocessor and analog input and output can have their I/O checked out with the addition of analog switches that wrap the output around to the input during self test. The microprocessor serves as a test controller, stimuli generator and response comparator enabling a check out of output devices by reading the signal with the input device.

4.2 ELEMENTS OF BIT LIBRARY (DATA BASE) FILES

All of the techniques of the Library package contain information in a standardized set of elements. The data elements consist of text files, lists, tables, graphic images and equations. This data is used by the CAD-BIT algorithm for tutorial presentations, BIT selection and BIT implementation. Figure 4-1 depicts the structure of a library element <L.E.> (BIT Technique) and the associated data elements for each library element. With reference to the figure, each Library Element contains 4 major categories of data:

- SHORT TUTORIAL
- LONG TUTORIAL
- USER REQUESTED DATA
- FIGURE OF MERIT EQUATIONS

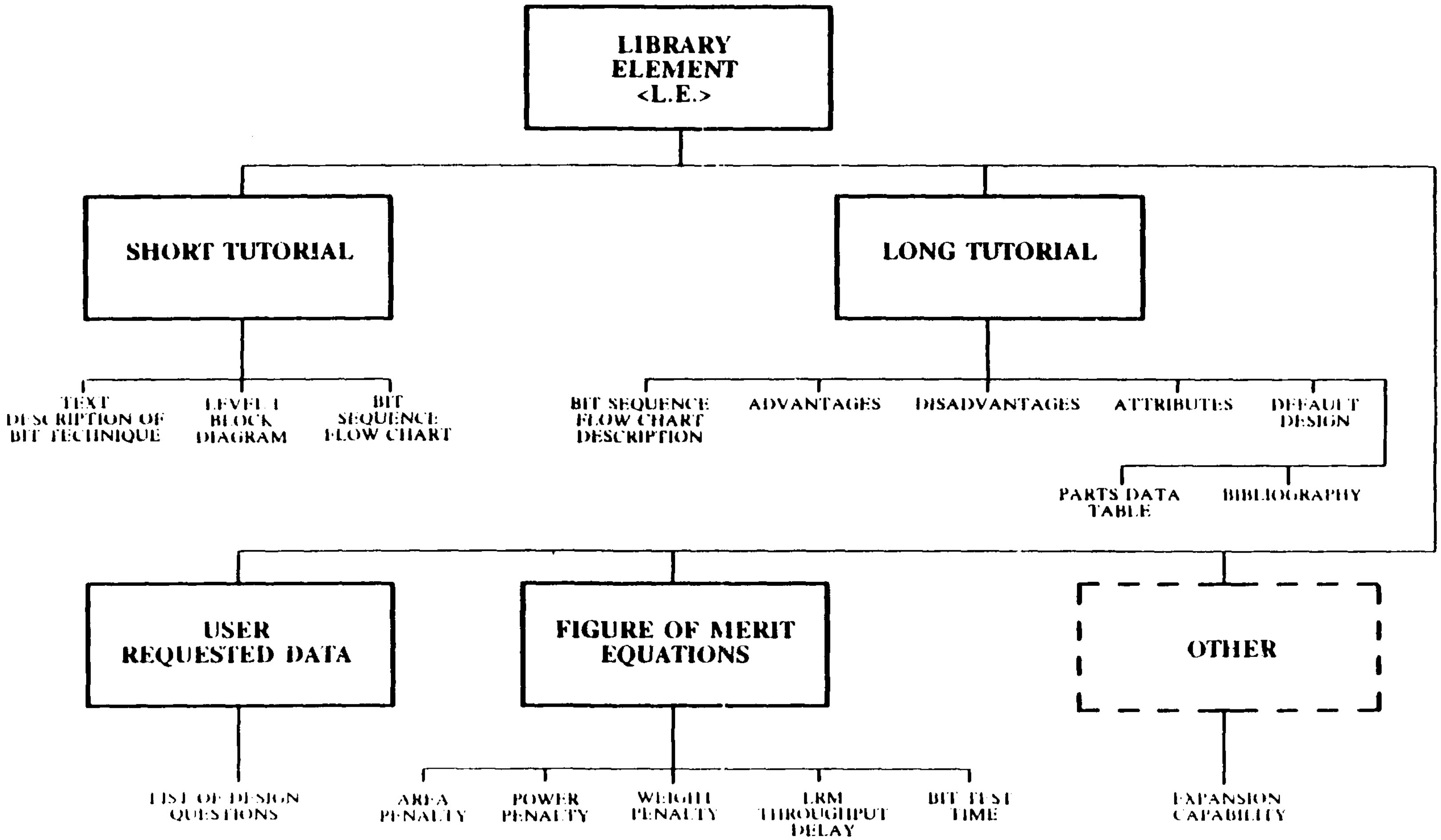


FIGURE 4–1
STRUCTURE OF THE CAD–BIT LIBRARY ELEMENT

Each category contains one or more subcategories of data. The following sections describe the contents of each sub category data element(s).

4.2.1 SHORT TUTORIAL

The Short Tutorial categories contains three single screen presentations designed to give a brief overview of the technique. The designer can scan through these tutorials to get acquainted with possible techniques for his application or to review the contents of the data base. The data presented is depicted in Figure 4-2.

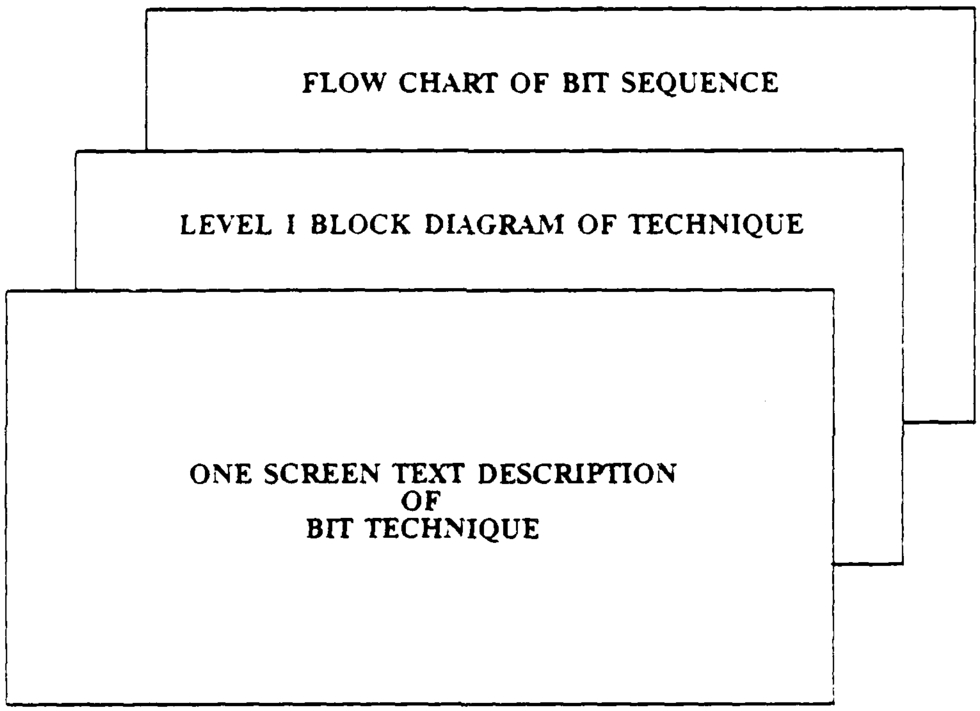


FIGURE 4-2
SUBCATEGORIES (DATA ELEMENTS) OF THE SHORT TUTORIAL

4.2.2 LONG TUTORIAL

The Long Tutorial Category provides more in depth material to help the designer become better acquainted with individual techniques. There are seven subcategories of data associated with this category and are illustrated in Figure 4-3. In the figure they are shown as a simple page but in actuality they may contain more than one page (or screen). The first subcategory is a description of the BIT sequence flow chart of the short tutorial. The detailed information of the next three sub categories is provided in a structured form rather than descriptive text. For example, there are separate tables for advantages, disadvantages and list of attributes.

A standard list of BIT attributes was identified and appropriate remarks for each attribute are indicated on all of the BIT techniques. The standardized attribute format was designed to facilitate comparisons of various techniques by the designer.

Following the attributes is the default design subcategory and the default design parts table. The purpose of this design is two-fold, first to provide a designer with a more detailed understanding of a particular BIT technique and secondly to provide a basis for estimating the real estate, power, weight and timing penalties. In most cases, the default design is only one configuration of many different possibilities. The design is approximate and for guidance only. The final design may have to contain many refinements such as decoupling capacitors, buffering to account for circuit loading, and part substitutions for those shown in the detailed design.

The last subcategory in the Long Tutorial is the Bibliography.

4.2.3 USER REQUESTED DATA

The User Requested Data category has only one subcategory, a list of questions to the user. Typical questions in this set are "How many primary inputs does the Circuit Under Test (CUT) have?", or "What is the test pattern applications rate?".

The answer for these questions is used to determine the amount of circuitry and the test time required by the BIT circuits.

4.2.4 FIGURE OF MERIT EQUATIONS

Figure of Merit Equations are used to calculate the real estate, weight, power and timing penalties. The equations for any given technique are based on the default design. However, since the actual circuit may have more or less I/O than the default design, the Figure of Merit equations must be adjusted to the actual CUT I/O. The adjustment information is obtained from questions posed to the designer. The questions are defined in the

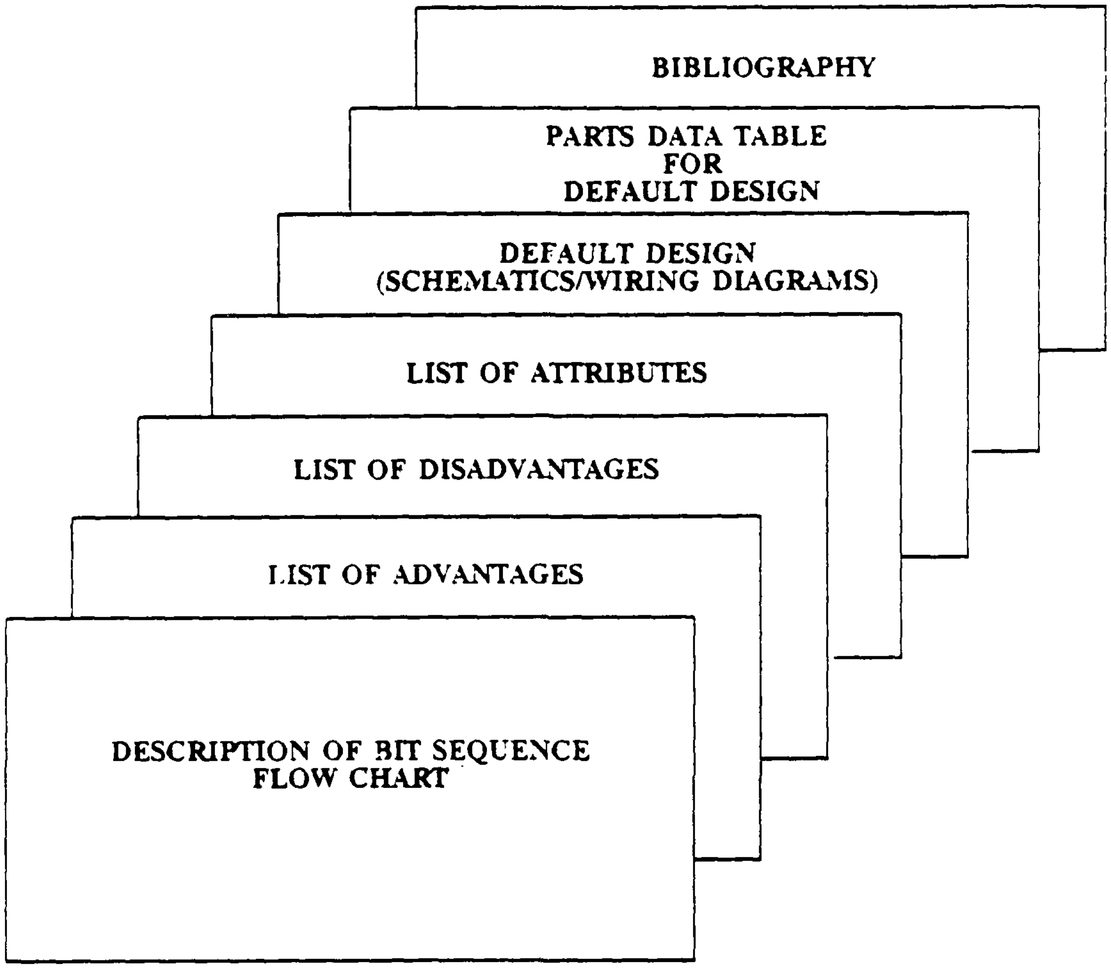


FIGURE 4-3
SUBCATEGORIES (DATA ELEMENTS) OF THE LONG TUTORIAL

User Requested Data category of section 4.2.3. Unlike the other elements of the library, the equation data elements are not displayed but are used internally within the CAD-BIT algorithm. The equation data is divided into the following three groups:

- VARIABLE DEFINITION
- COMPONENT DETERMINATION EQUATION
- PENALTY EQUATIONS

5.0 DRAWING CONVENTIONS

Many of the drawings show a mixture of CUT circuitry and BIT circuitry. The shaded blocks in the block & circuit diagrams represent CUT circuit, while the unshaded blocks represent BIT circuitry.

6.0 CAD-BIT DATA BASE

The CAD-BIT data base presently has nine digital, three analog and one hybrid techniques in its library. Additional techniques can be easily added to the data base. The CAD-BIT data base structure is illustrated in Figure 6-1. This volume contains the data for the BIT Technique Files only. The CAD-BIT System Files data is found in Volume III, CAD-BIT Specification. Design Related Data Files are generated by CAD-BIT when CAD-BIT is in operation.

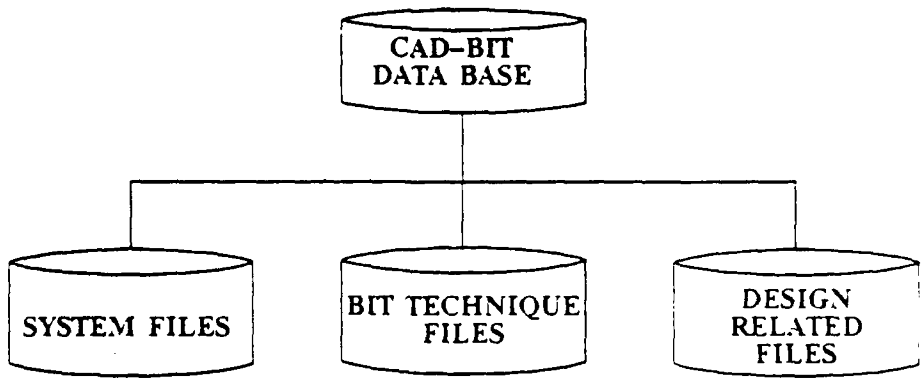


Figure 6-1

CAD-BIT DATABASE OVERVIEW

PARAGRAPH 6.1

ON-BOARD ROM TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM

CATEGORY: SHORT TUTORIAL

SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE

DATA TYPE: TEXT [X] LIST [ ] TABLE [ ] GRAPHIC [ ] EQUATIONS [ ]

DATA:

SHORT TUTORIAL FOR ON-BOARD ROM

On-Board Read Only Memory (ROM) Self Test is non-concurrent, mostly hardware and firmware, Built-In-Test (BIT) technique which consists of applying test patterns that are stored in an on board ROM to a Circuit Under Test (CUT) and then comparing the CUT's response to what is expected, resulting in a go - no/go output signal. Although the number of test patterns required to exhaustively test a function is proportional to the cube of the number of gates, this technique has some potential in that each test pattern can be individually and selectively determined, thereby, maximizing the percentage of fault detection to the test pattern ratio.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM	
CATEGORY: SHORT TUTORIAL	**PAGE** 2 **of** 4
SUBCATEGORY: 1. LEVEL I BLOCK DIAGRAM. 2. BIT SEQUENCE FLOW CHART.	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2

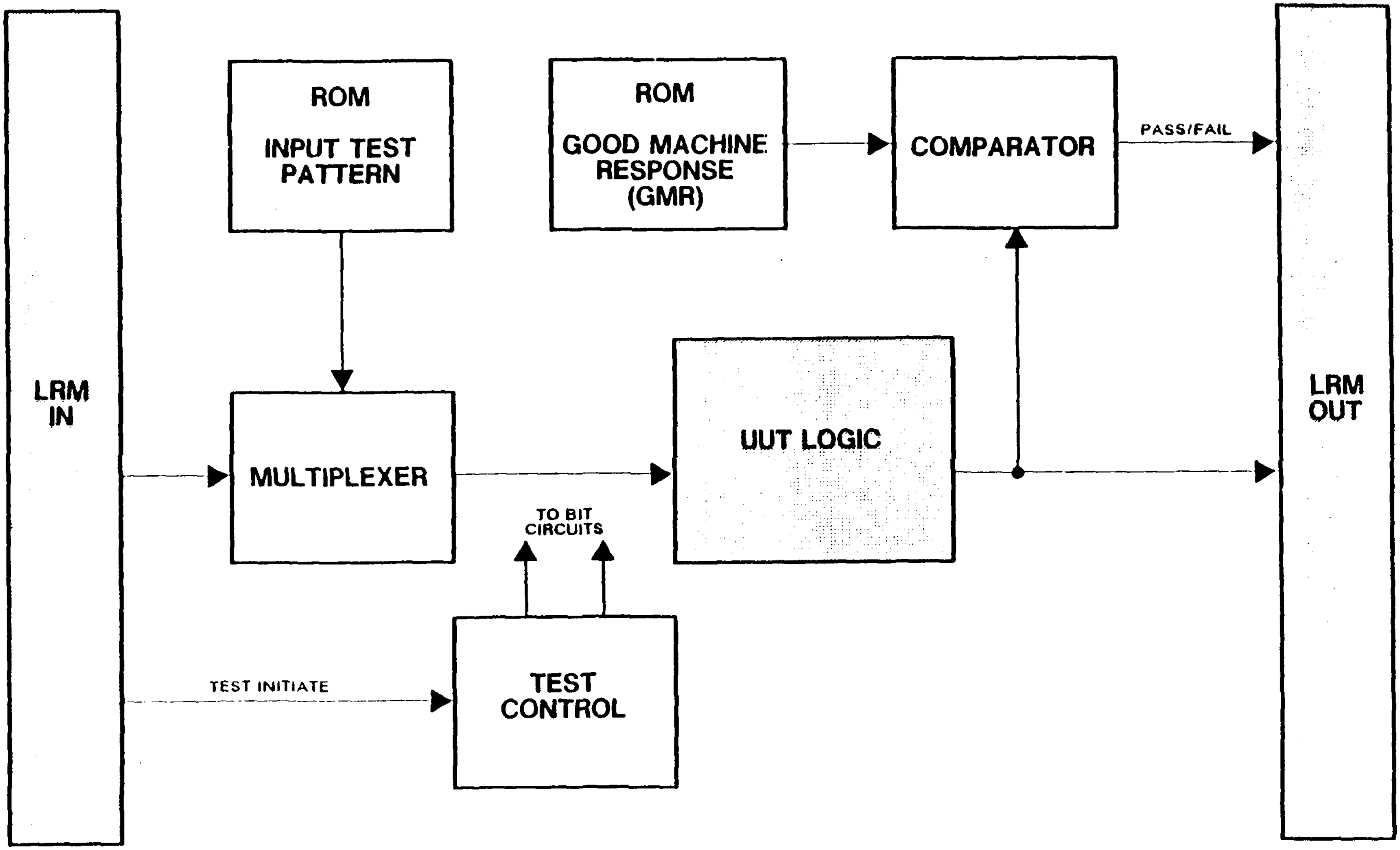


FIGURE 1 – LEVEL I BLOCK DIAGRAM FOR ON-BOARD ROM

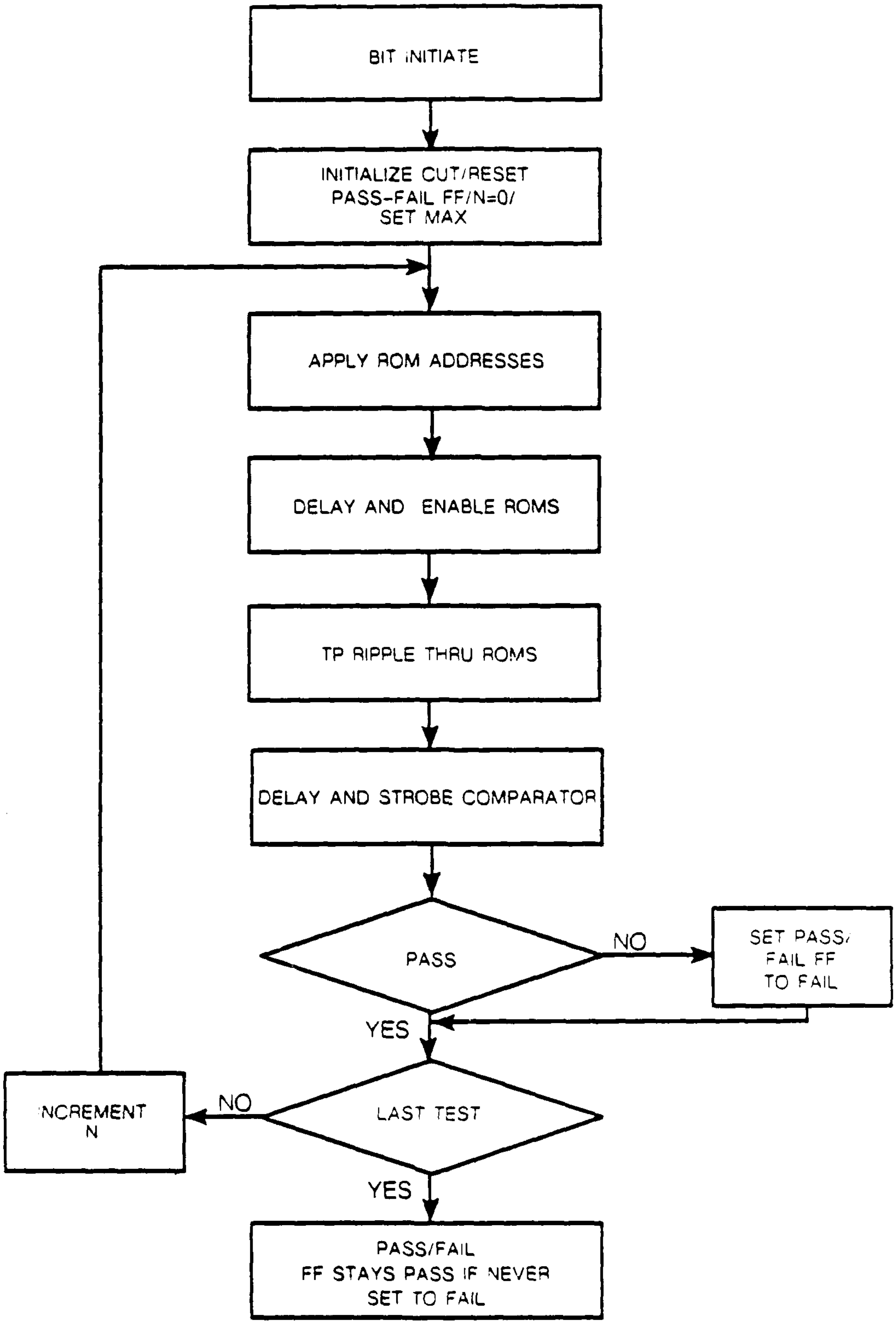


FIGURE 2 – BIT SEQUENCE FLOW CHART FOR ON-BOARD ROM

PAGE 4 of 4

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION FOR ON-BOARD ROM

1. A positive pulse "Test Initiate" signal is input to test control logic to begin test.
2. The test begins as follows:
   - "BIT Mode" signal from control logic to multiplexer is activated
   - Normal inputs to CUT multiplexed out
   - Test Patterns (TP) from TP ROM input to CUT enable
   - All resettable logic of CUT reset
   - ROM address counter in control logic reset to zero
   - "Pass/Fail" Flip-Flop (FF) in comparator logic block reset to "Pass"
3. The system clock, while in BIT mode, increments the control logic counter which addresses the TP & Good Machine Response (GMR) ROMs simultaneously.
4. After a delay sufficient to fully establish the addressing in the step above, both the TP & GMR ROMs are enabled.
5. The TP ripples through the CUT. To gain control of the CUT clock, each TP will have both high and a low on the clock line which may come from the TP ROM
6. After enough delay for a good machine to establish a GMR at the CUT's outputs, the comparator is enabled.
7. A good machine at this time will have the GMR pattern identically compare with the CUT outputs. If not, the Pass/Fail FF will be set to "Fail" and will remain "Fail" until BIT is re-initiated.
8. If the address to the ROMs is the last address, then "End Of Test" control logic signal goes low. The moment the enable comparator signal goes HI during this last TP sequence, the BIT mode FF is reset and the system is out of BIT mode. The Pass/Fail FF will remain set to "Pass" if during the test it was never set to "Fail".
9. If not the last ROM address, go back to step 3.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ON-BOARD ROM BIT
ADVANTAGES

1. An understanding of the CUT can lead to a substantial percentage of fault detected with a few, determined test patterns.

2. A CUT with much sequential logic requires specific "Pairs" of test patterns applied in sequence. Although, this presents a problem with Random Test Pattern Application, storing the test patterns in ROM so that they indeed do occur in pairs is done without difficulty with the On-Board ROM Method.

3 On-Board ROM Test Generation becomes competitive when compared to random pattern generation as the number of CUT inputs become large and/or number of patterns required becomes small. This is best understood by considering that the total number of binary patterns possible for a CUT with n inputs is 2^n. If n=16, 2^n = 65,536. If n=20; 2^n = 1,048,576. If n=24; 2^n = 16,777,216. Consider a hypothetical 24 input CUT that can be adequately tested with 2,000 deterministic patterns. Most of the Test Pattern Generator (TPG) hardware required using On-Board ROM Method are cascaded, 2K by 8 ROMs as compared to 3 cascaded, 8-Bit shift registers plus 2 Quad Exclusive Or Packages. But the real savings is test time. To be absolutely sure of providing all 2,000 test patterns one must cycle through 16,777,215 possible test patterns when using random pattern generator.

4 The control logic for the On-Board ROM Test is simple when compared to the Random Test Pattern Generation method which requires loading seed patterns and special test sequencing.

5 Read control logic and address and data buses may possibly be shared between test and function purposes.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM BIT

CATEGORY: LONG TUTORIAL | **PAGE** 3 **of** 14

SUBCATEGORY: BIT TECHNIQUE DISADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ON-BOARD ROM BIT
DISADVANTAGES

1. With the growing complexity of electronic circuitry being implemented on Line Replaceable Modules (LRM) of today, it is becoming more and more difficult for a test engineer to understand what he is testing, especially when under pressure to establish the test plan quickly. Without a true understanding of what is to be tested, it is nearly impossible to effectively and efficiently determine the test patterns that are necessary.

2. When the number of test patterns required to obtain adequate fault coverage is large and/or the number of CUT inputs is small or can be partitioned into a few small number of input groups, then the real estate required for the On-Board ROM Method becomes excessive when compared to the random pattern generation method.

3. Memory elements in general are not as reliable as random logic microelectronic devices.

4. Circuit design changes often require reprogramming the ROMs.

5. If the number of bus lines required to address the ROMs are excessive and/or the distance between the TP ROMs and the control logic, or between the GMR ROMs and the control logic is substantial, then Printed Circuit Board (PCB) real estate consumed is excessive and costly.

6. Memory allocated to either store test patterns or GMRs can never serve both test and function purposes as can shift registers used in Built in Logic Block Observers (BILBO) for example.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ON-BOARD ROM BIT
ATTRIBUTES

1. REAL ESTATE PENALTY
   - Increases with CUT complexity
   - ROMs - Number of test patterns is approximately the cube of the number of gates for combinational. FFs increase the number even further
   - Control - Approximately 11 chips for this example. Number of counter chips increases with number of test patterns
   - Multiplexer - Number multiplexer chips equals number input lines divided by number of lines switched by multiplexer chip
   - Comparator - Number comparator chips equals (number output lines) divided by number of lines compared by chip
   - Land real estate depends on layout

2. POWER PENALTY
   - Roughly proportional to real estate penalty example:
     Power Penalty equals Percent Real Estate Penalty multiplied by CUT Normal power.
     - Exceptions (some ROMS have power down mode)
     - Switch Technology (use Metal Oxide Semiconductors (MOS) ROMS for higher density)

3. RELIABILITY PENALTY
   - Proportional to Real Estate Penalty if similar technology is used for Built in Test Equipment (BITE) as for CUT
   - May have to distinguish BITE failures that only effect BITE vs BITE failures that effect CUT
   - Computer Aided Design (CAD) System may have software package for reliability calculation

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM	
CATEGORY: LONG TUTORIAL	PAGE 5 of 14
SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ON-BOARD ROM BIT
ATTRIBUTES
(CONT)

4. TIMING PENALTY
   - Test Time Duration - Number of Test Patterns multiplied by Pattern Application Period
   - Circuit throughput Delay - Additional delays of Multiplexers
5. NON-CONCURRENT
6. CONCEPTUAL COMPLEXITY
   - Straight Forward
7. HARDWARE/SOFTWARE
   - Test Patterns in Firmware
8. TECHNOLOGY
   - All current digital technologies
   - May use higher density technologies for ROM to reduce real estate penalty. (May need MOS-Transistor Transistor Logic (TTL) converters)
9. IS BITE SELF TESTABLE?
   - Can do check sum on ROMs (add hardware)
   - Some ROMs have shadow registers
10. DESIGN COST
   - Use standard estimating procedures based on number of chips
   - Must add Engineering time to create Test Patterns and GMRs
   - May need debug time to hardware verify proper operation

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ON-BOARD BIT ROM
ATTRIBUTES
(CONT)

11. SOFTWARE DESIGN COST
    - Only applicable at system level

12. NUMBER OF BYTES OF STORAGE REQUIRED
    - Function of complexity of circuit (see Real Estate Penalty)

13. STAND-ALONE (SELF-CONTAINED BIT)?
    - Yes

14. WEIGHT
    - Proportional to real estate penalty weight
    - PENALTY = (Percent Real Estate Penalty) x (Weight of circuit)

15. Commercially available integrated circuits with testability features ROMs are available with shadow registers.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM	
CATEGORY: LONG TUTORIAL	**PAGE** 7 **of** 14
SUBCATEGORY: DEFAULT DESIGN	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

a) See figure 3 for ON-BOARD ROM LEVEL II BLOCK DIAGRAM.

b) See figure 4 for TEST PATTERN AND GOOD MACHINE RESPONSE ROM DEFAULT DESIGN.

c) See figure 5 for GOOD MACHINE RESPONSE COMPARISON LOGIC DEFAULT DESIGN.

d) See figure 6 for INPUT MULTIPLEXER DEFAULT DESIGN.

e) See figure 7 for CONTROL LOGIC FOR ON-BOARD ROM DEFAULT DESIGN.

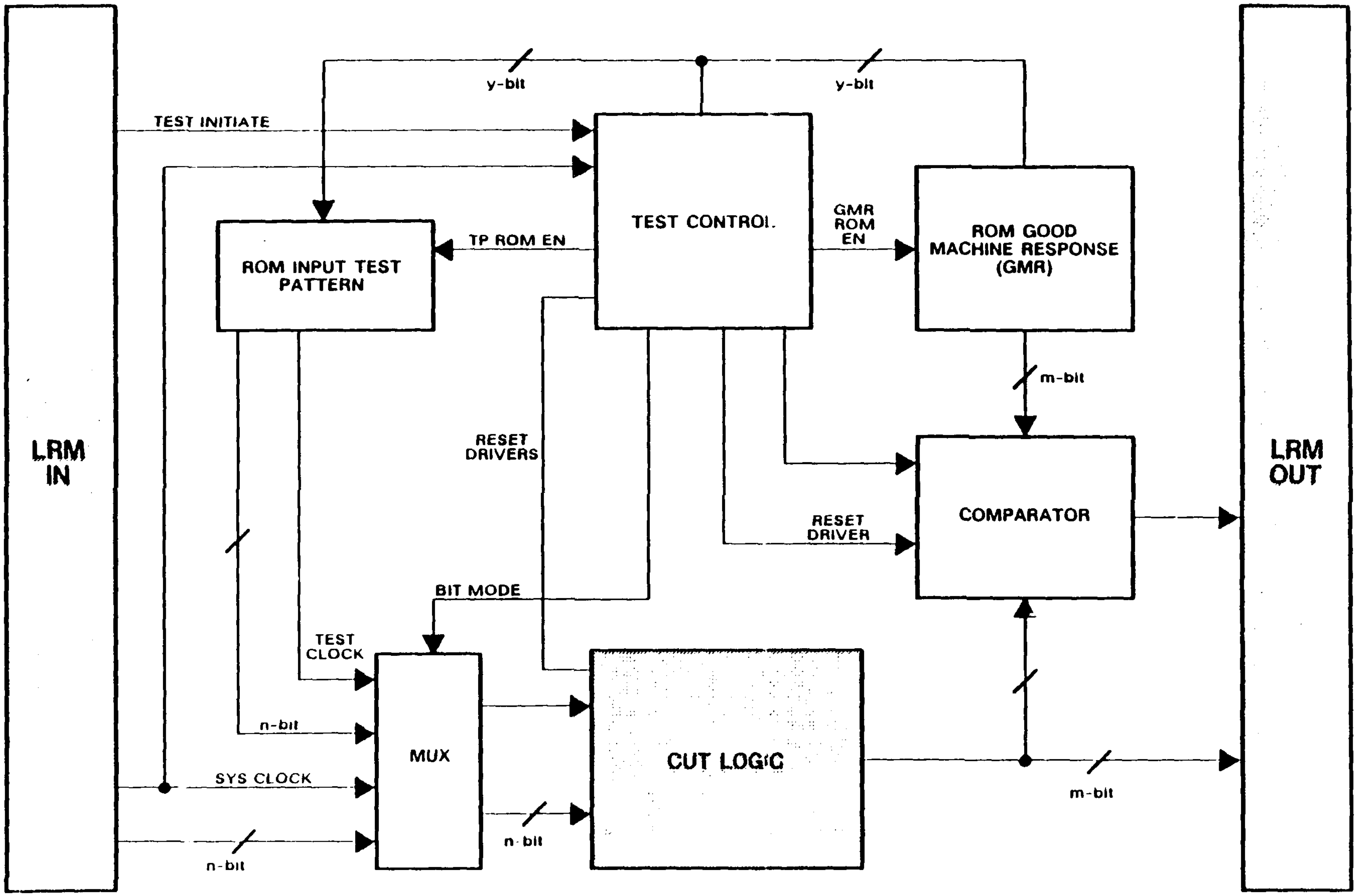


FIGURE 3 ON-BOARD ROM LEVEL II BLOCK DIAGRAM

PAGE 8 of 14

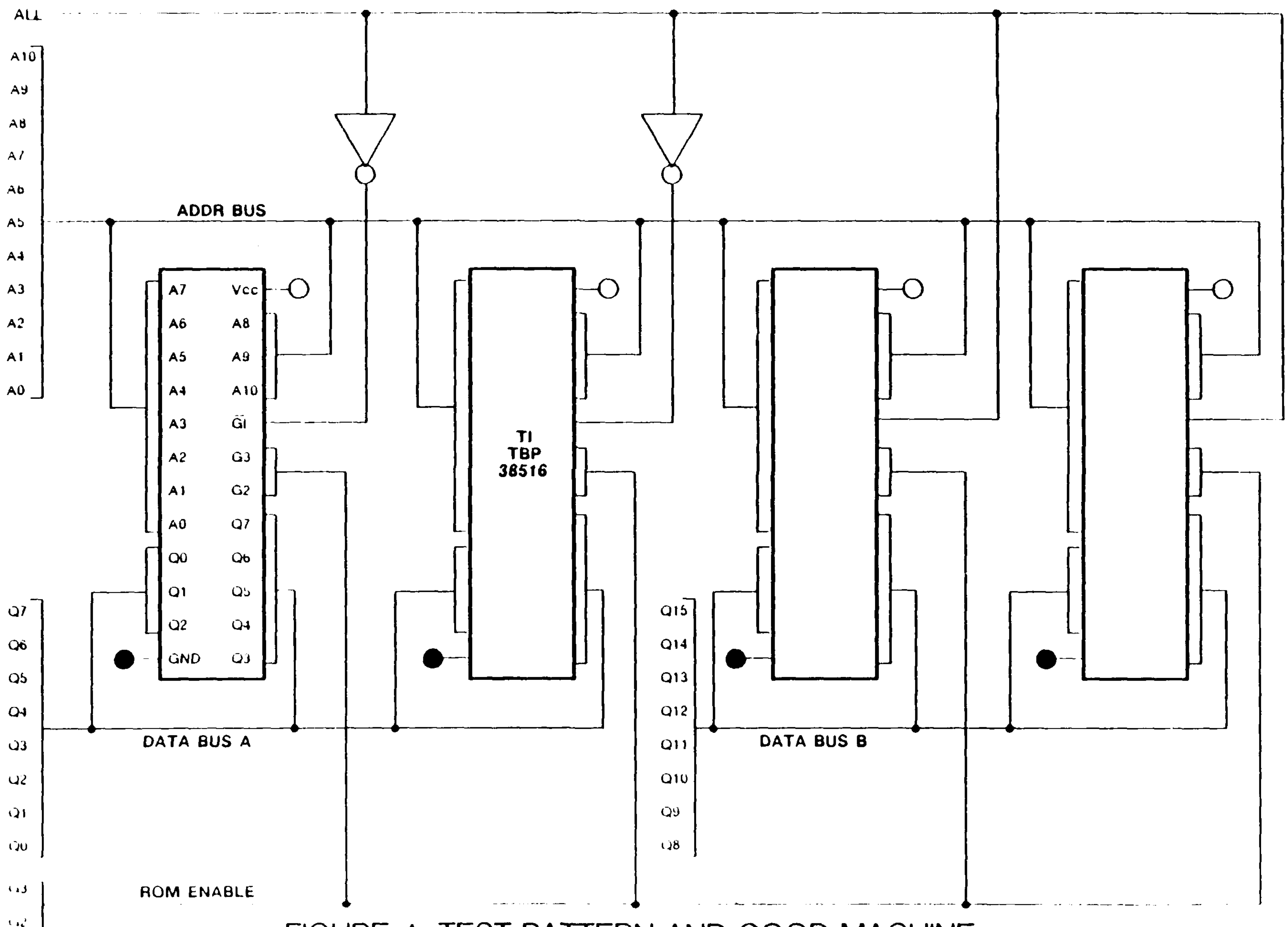
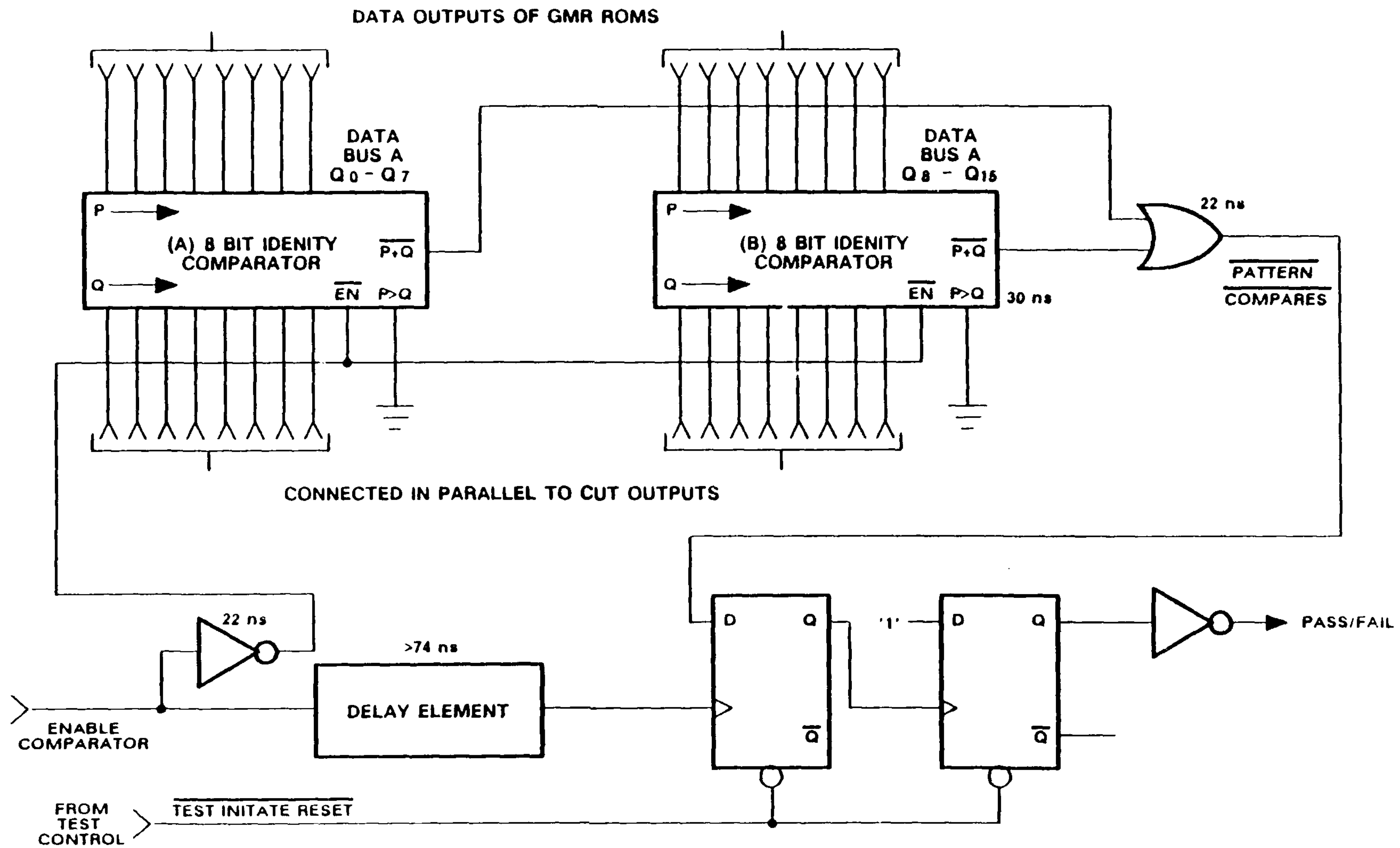
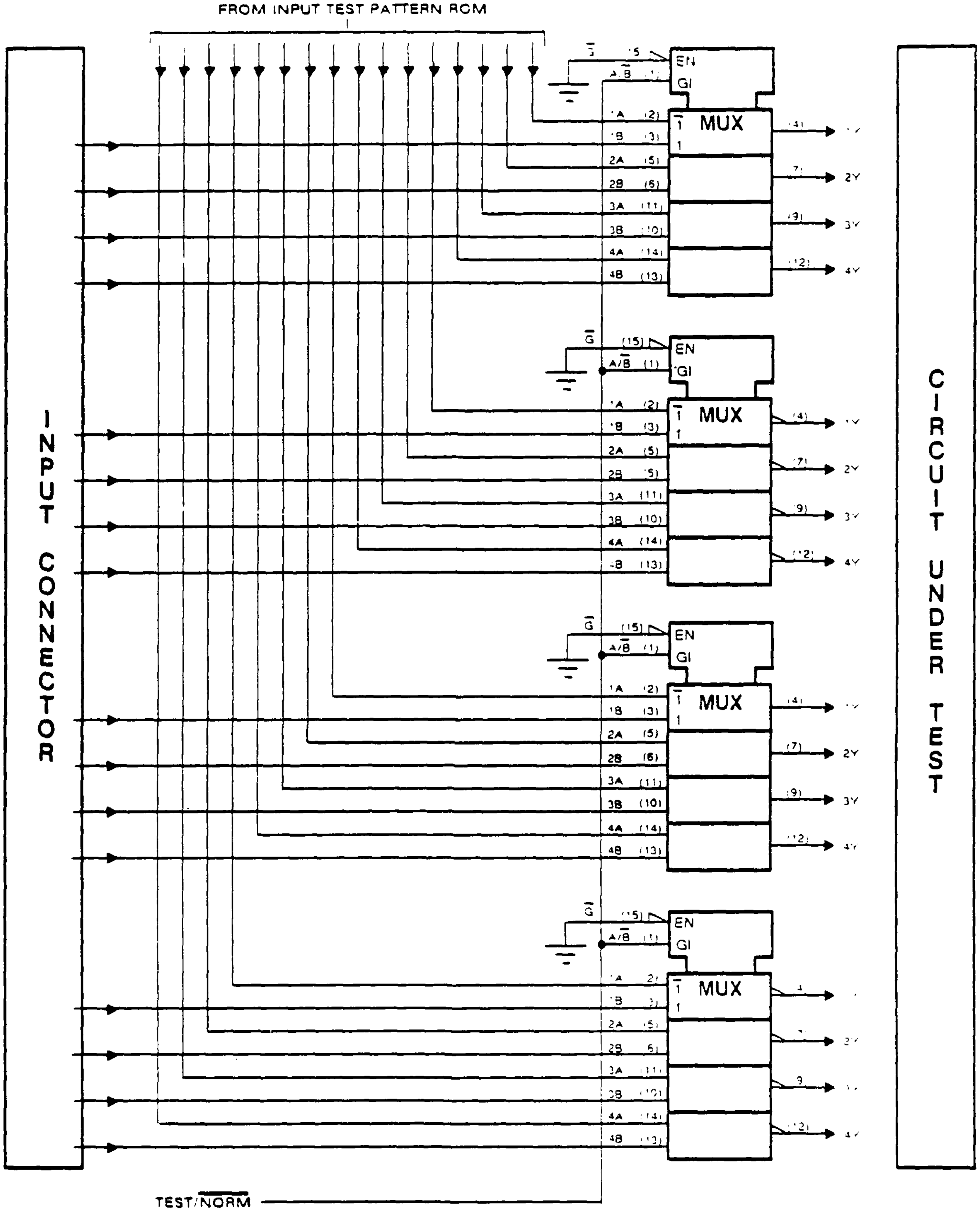


FIGURE 4 TEST PATTERN AND GOOD MACHINE RESPONSE ROM



ns nanosecond delay

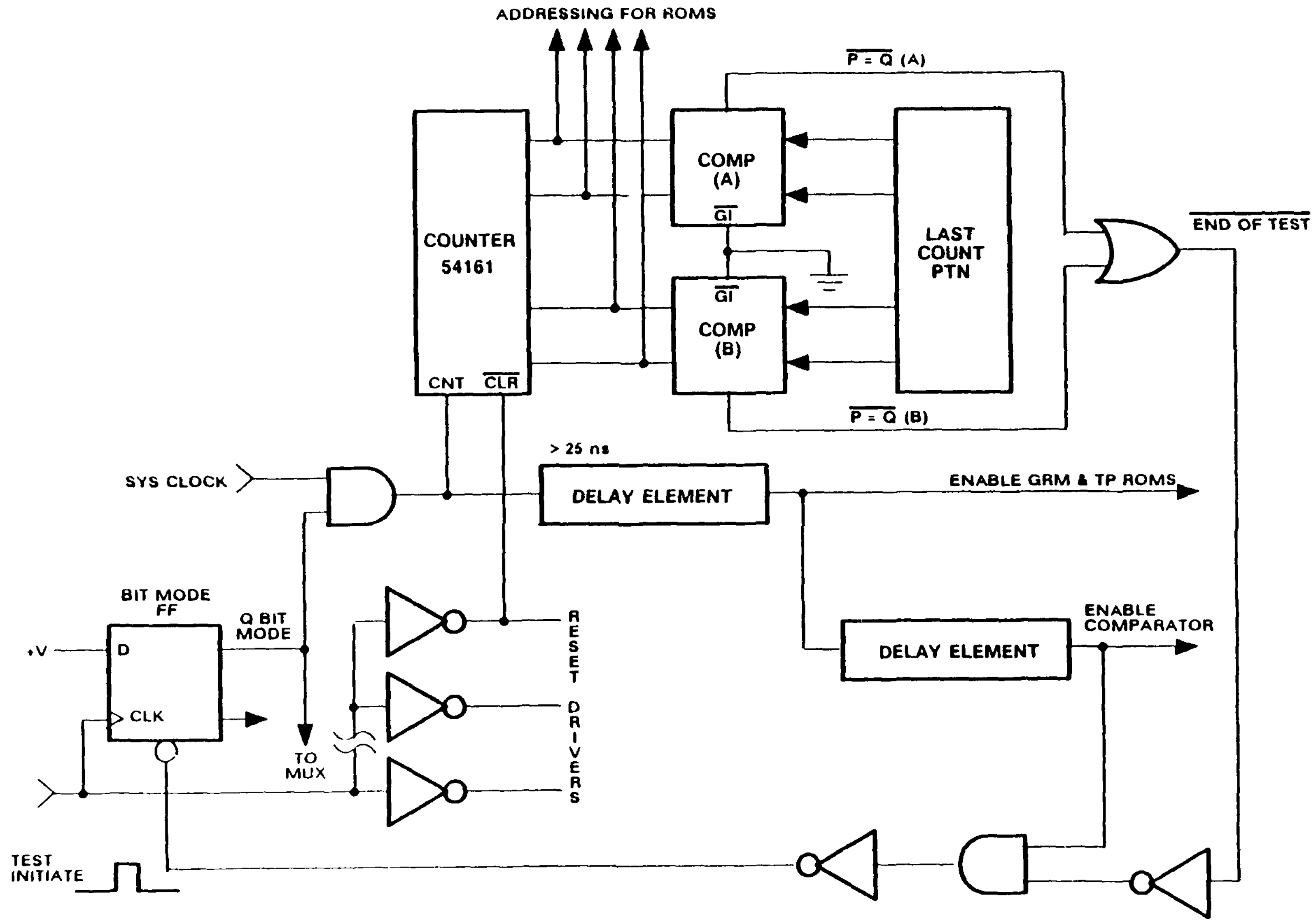
FIGURE 5 GOOD MACHINE RESPONSE COMPARISON LOGIC



NOTE: 2 QUAD 2 TO 1 LINE DATA SELECTOR/MUX's CAN BE REPLACED BY AN OCTAL 2 INPUT MUXED LATCH-LS604.

FIGURE 6 INPUT MULTIPLEXER

PAGE 11 of 14



ns nanosecond delay

FIGURE 7 CONTROL LOGIC FOR ON-BOARD ROM

PAGE 12 of 14

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM

CATEGORY: LONG TUTORIAL | **PAGE** 13 **of** 14

SUBCATEGORY: PART DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

ON-BOARD ROM
PART DATA TABLE

NUMBER/NAME	AREA *(sq in)*	# OF PINS	POWER TYPICAL *(mW)*	POWER MAX. *(mW)*	WEIGHT *(gms)*
TBP385L16 2K x 8 PROM	0.375	24	325	500	6.5
74LS604/ OCT 2-IN MUXs LATCHES	0.87	28	275	350	7.5
74LS686/ 8 BIT MAG/ IDENT COMP	0.375	24	220	375	6.5
741617/ 4 BIT SYNC BIN COUNTER	0 243	16	315	455	2
7404/ HEX INVERTERS	0.243	14	90	165	2
7400/ QUAD 2-IN POS NAND	0.243	14	60	110	2
74125/ QUAD D FLIP FLOP	0.243	16	55	90	2

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM	
CATEGORY: LONG TUTORIAL	PAGE 14 of 14
SUBCATEGORY: BIBILOGRAPHY	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

NONE REQUIRED

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM

CATEGORY: USER REQUESTED DATA

PAGE 1 **of** 1

SUBCATEGORY:

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

QUESTIONS	VARIABLE ASSIGNMENT
1. How many primary input pins are used by the PCB's operational circuitry?	v1
2. How many primary output pins are used by the PCB's operational circuitry?	v2
3. How many test patterns are required to be stored in the ROMs?	v3
4. What is the test pattern application rate?	v4
5. What is the estimated initialization time?	v5

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM

CATEGORY: EQUATIONS | **PAGE** 1 **of** 2

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITIONS

n1= Number of ROM chips
n2= Number of MUX chips
n3= Number of COMPARATOR chips
n4= Number of COUNTER chips
n5= Number DECODE chips
n6= Number of PROGRAMMABLE DELAY chips
n7= BIT MODE status FF
n8= Number of CONTROL GATES
v1= Number of INPUT PINS<= 120
v2= Number of OUTPUT PINS<= 120
v3= Number of TEST PATTERNS<= 12288
v4= PATTERN RATE
v5= INITIALIZATION TIME

II) COMPONENT DETERMINATION EQUATIONS

n1= (v1/8)*(v3/2048) + (v2/8)*(v3/2048)
n2= (v1/8)
n3= (v2/8)
n4= (v3/16)
n5= Integer of ((n4 + 1)/2)
n6= 2
n7= 1
n8= 2

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD ROM

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

III) PENALTY EQUATIONS

a) AREA (sq in)

Area of BIT chips = (.375)n1 + (.87)n2 + (.375)n3 + (.243)n4 + (.375)n5 + (.375)n6 + (.243)n7 + (.243)n8

Total area of BIT circuitry = (Area of BIT chips) + 15% for PC traces = 1.15 (Area of BIT chips)

b) POWER (mW)

Power = (325)n1 + (350)n2 + (375)n3 + (455)n4 + (375)n5 + (200)n6 + (90)n7 + (110)n8

c) WEIGHT (gms)

Weight of BIT chips (grams) = (6.5)n1 + (7.5)n2 + (6.5)n3 + (2.0)n4 + (6.5)n5 + (6.0)n6 + (2)n7 + (2)n8

Weight of BIT circuitry = Weight of BIT chips + 10% For Weight of solder = 1.1 (Weight of chips)

d) TIME (ns)

Test time = (v3) (v4) + v5

Throughput delay = 30

PARAGRAPH 6.2

MICROPROCESSOR BIT TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: SHORT TUTORIAL

SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE

DATA TYPE: TEXT [X] LIST [ ] TABLE [ ] GRAPHIC [ ] EQUATIONS [ ]

DATA:

SHORT TUTORIAL FOR MICROPROCESSOR BUILT-IN-TEST

Microprocessor Built-In-Test (BIT) is accomplished using functional fault models which comprehensively, and efficiently test the microprocessor. To implement this method, some test program memory, and the built-in intelligence of the microprocessor are required. An optional external test module may also be used, depending on the microprocessor being tested. The external test module is a device controlled by the Central Processing Unit (CPU) and is used to control or initiate microprocessor peripheral control devices which are located on the microprocessor chip.

Microprocessor BIT is done in stages. Each subsequent stage builds upon the successful completion of prior stages. These stages are performed in the specific order shown below:

- Core instruction tests
- Read register Instruction tests
- Memory tests
- Addressing Modes tests
- Instruction Execution tests
- Instruction Sequence tests
- I/O peripheral controller tests

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: SHORT TUTORIAL

SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE

DATA TYPE: TEXT [X] LIST [ ] TABLE [ ] GRAPHIC [ ] EQUATIONS [ ]

DATA:

SHORT TUTORIAL
FOR
MICROPROCESSOR BUILT-IN-TEST
(CONT)

In addition to the microprocessor, the external test module may optionally be tested. It is tested in the following manner:

- Verify CPU is operating properly (see above list).
- Set up on-chip peripheral controllers in external control mode.
- Use the external test module to set up external on-chip peripheral controller requests.

Normally, Microprocessor BIT is executed at the operating speed of the microprocessor.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST	
CATEGORY: SHORT TUTORIAL	PAGE 3 of 6
SUBCATEGORY: 1. LEVEL I BLOCK DIAGRAM 2. BIT SEQUENCE FLOW CHART	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2

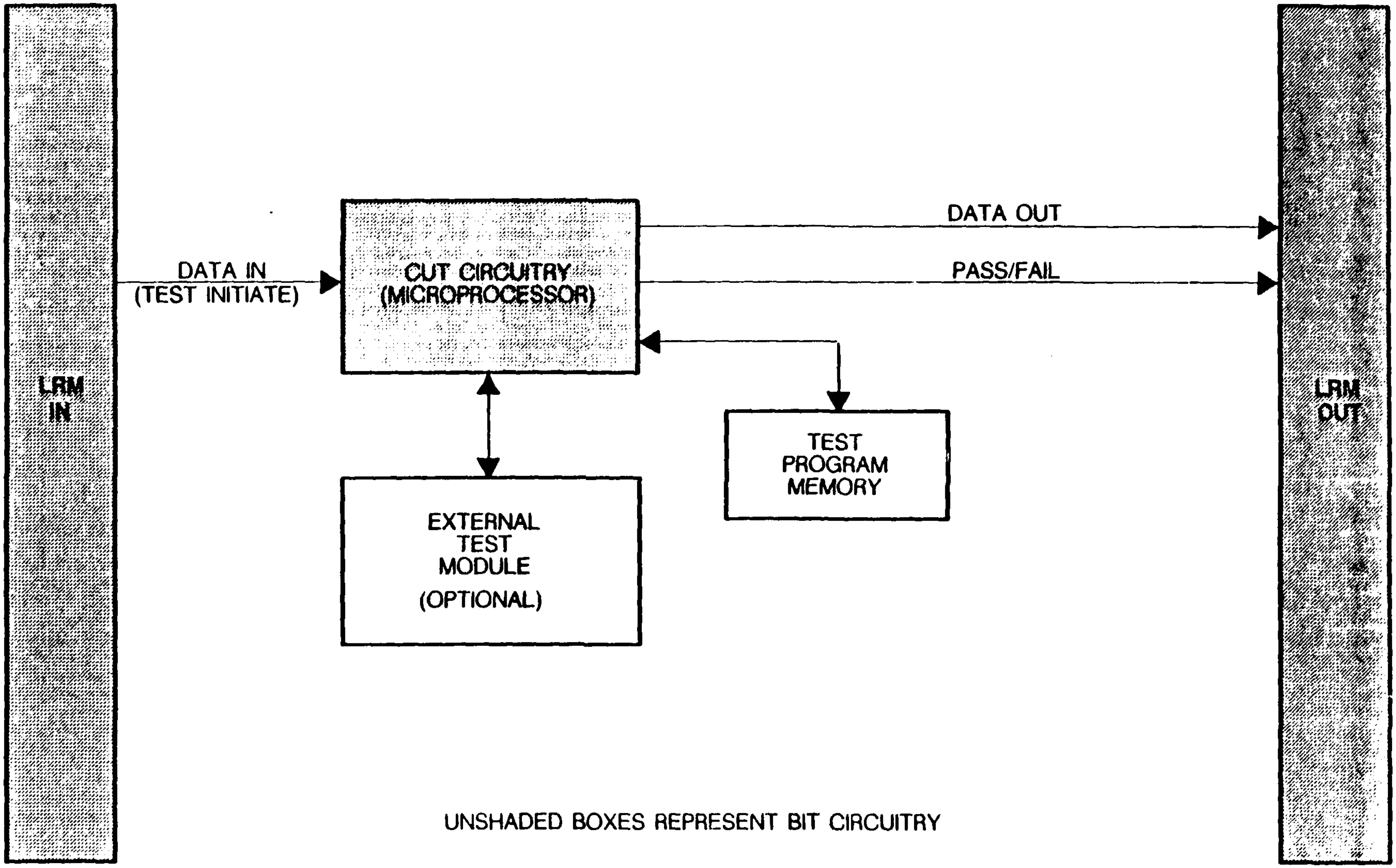
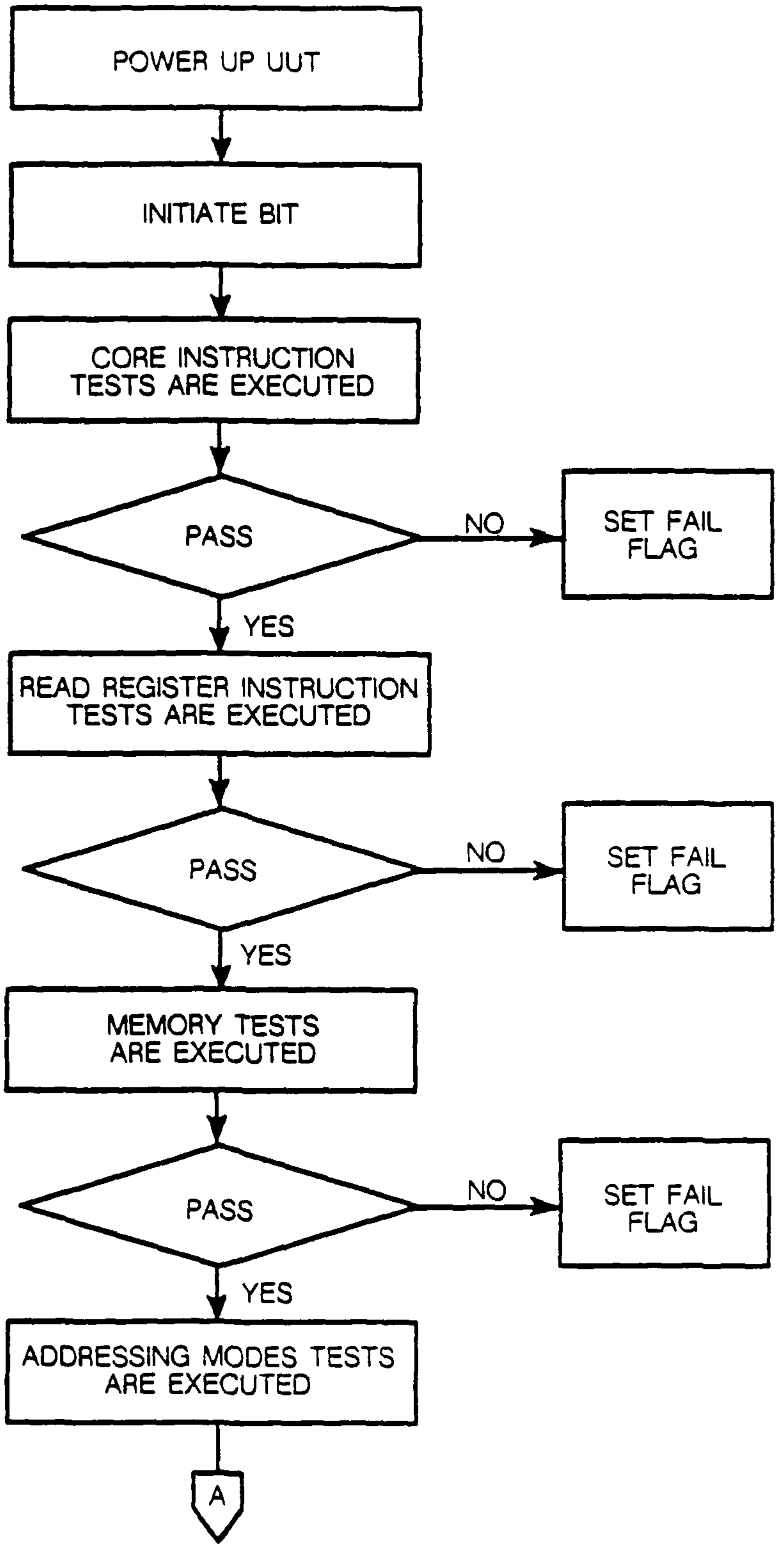


FIGURE 1 LEVEL I BLOCK DIAGRAM FOR MICROPROCESSOR BIT



SEE NEXT PAGE

FIGURE 2 BIT SEQUENCE FLOW CHART FOR MICROPROCESSOR BIT

PAGE 5 of 6

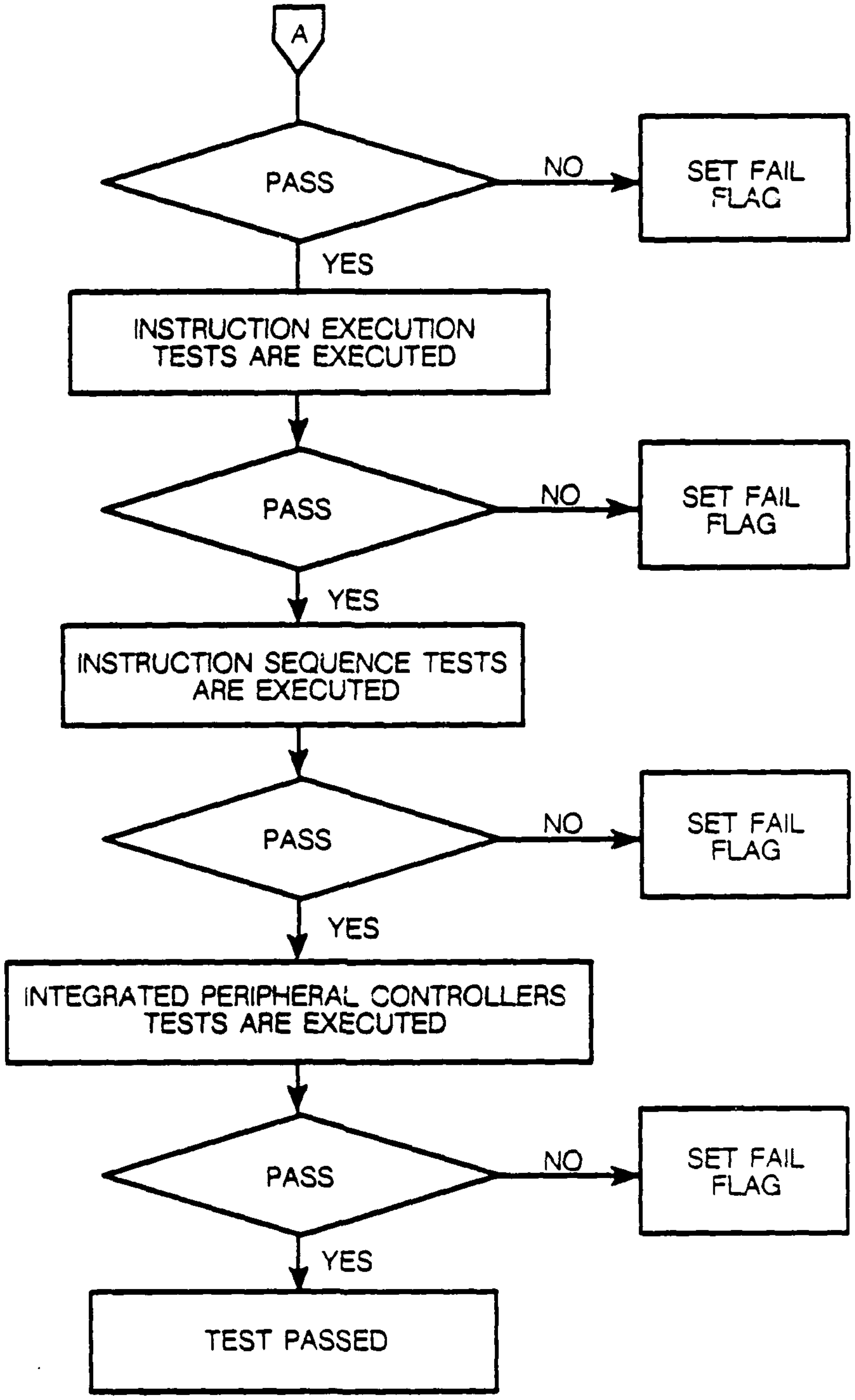


FIGURE 2 BIT SEQUENCE FLOW CHART
FOR MICROPROCESSOR BIT
(CONT)

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
FOR
MICROPROCESSOR BUILT-IN-TEST

1. Unit Under Test (UUT) is powered up.
2. An initiate BIT signal is generated.
3. A procedure is executed which verifies the proper operation of the MOVE, COMPARE and BRANCH instructions. These instructions are typically defined as follows:
   - MOV a, Ri: Load register Ri with the contents of memory location a.
   - CMP Ri, Rj: Compare the contents of Ri to Rj and set the Z bit if Ri = Rj.
   - BEQ a: If the Z bit of the Status Register (SR) is set then branch to location a.

   These instructions must be operational before any further testing can proceed because they are a kernel which enables testing the execution of further instructions in the instruction repertoire.

4. If a fault is detected in the Core instructions test, a failure flag is set and testing is terminated. If no faults are detected, testing will proceed to the Read Register instruction tests.

5. A procedure is executed which verifies proper execution of the Read Register instructions of the microprocessor. The procedure verifies that the proper data is read and checks for simple faults.

6. If a fault is detected, a failure flag is set. If no faults are detected, testing will proceed to the Memory test.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
FOR
MICROPROCESSOR BUILT-IN-TEST
(CONT)

7. A procedure is executed which verifies proper operation of the memory chips.

8. If a fault is detected, a failure flag is set. If no faults are detected, testing will proceed to the Addressing Modes tests.

9. A procedure is executed which verifies proper loading of registers in all the addressing modes of the microprocessor. This verifies that all addressing modes are functional.

10. If a fault is detected, a failure flag is set. If no faults are detected, testing will proceed to the Instruction Execution test.

11. A procedure is executed which verifies that the Instruction Execution process is functional. This is accomplished by loading the registers with codewords, executing an Instruction set, and verifying the proper content of the registers.

12. If a fault is detected, a failure flag is set. If no faults are detected, testing will proceed to the Instruction Sequence test.

13. A procedure is performed where all possible ordered pairs of instructions are tested. Ordered pairs of instructions are defined as instructions which are commonly used together. The following faults are tested for:

    1. No data dependence (the sequence fault is independent of the operands used with the instructions).
    2. Pairwise instruction sequence dependence.

14. If a fault is detected, a failure flag is set. If no faults are detected, testing will proceed to the Integrated Controllers tests.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: LONG TUTORIAL

SUBCATEGORY: TEST SEQUENCE DESCRIPTION

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
FOR
MICROPROCESSOR BUILT-IN-TEST
(CONT)

15. In general, the fault model for any on-chip peripheral controller is as follows:
    1. Registers belonging to the peripheral control device have stuck-at faults. The result of these faults will be incorrect, or no execution of the device function.
    2. Faults in decoders of the peripheral control device cause incorrect, or no selection of peripheral control registers.
    3. Faults in the control logic of the peripheral causes an incorrect, or no execution of the controller function.
    4. A fault in the on-chip peripheral may cause a side effect in other areas of the microprocessor which may be detected in its readable registers.
16. If a fault is detected, a failure flag is set. If no faults are detected, the Microprocessor BIT passed.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

MICROPROCESSOR BIT ADVANTAGES

The Microprocessor BIT technique provides the following advantages to the circuit designer:

- The real estate penalty will be minimal, basically requiring Read Only Memory (ROM) locations which may be already available if there is spare ROM space after the design is complete. If an external test module is required, the real estate penalty will be slightly increased.
- Most of the testing done is executed at the operating speed of microprocessor.
- Monitoring of test results is carried out by the microprocessor itself.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE DISADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

MICROPROCESSOR BIT
DISADVANTAGES

The Microprocessor BIT technique poses the following disadvantages to the circuit designer:

- The test memory requirement for Microprocessor BIT can be large depending on the following factors:
    1. Characteristics of the microprocessor.
    2. Thoroughness of the tests.
    3. Optimization of test code for both fast test execution and compact test memory size.
- Most of the code must be written in assembly language to test the microprocessor which is not as readable as high level languages.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

MICROPROCESSOR BIT
ATTRIBUTES

1. REAL ESTATE PENALTY
   - The number of memory chips used is proportional to the total memory requirement of the self-test program used.
   - If an External Test Module is required, an additional real estate penalty will be accrued consisting of:
     a. Several registers
     b. Control logic circuitry

2. POWER PENALTY
   - Proportional to the number of memory chips.
   - If an External Test Module is required, an additional power penalty will be accrued.

3. RELIABILITY PENALTY
   - Proportional to the Mean Time Between Failures (MTBF) of the memory chips.
   - If an External Test Module is required, an additional reliability penalty will be accrued.

4. TIMING PENALTY
   - Proportional to the operating speed of the microprocessor and the length of the test program.

5. CONCEPTUAL COMPLEXITY
   - Circuit design is moderate in complexity.
   - Extensive software programming is required in assembly languages.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

MICROPROCESSOR BIT
ATTRIBUTES
(CONT)

6. TECHNOLOGY
   - Digital circuitry
7. IS BITE SELF TESTABLE?
   - Yes
8. DESIGN COST
   - All components used are readily available at low cost.
   - Software development time of the BIT programs stored in memory is proportional to the complexity and thoroughness of the tests used.
   - Hardware design and debug is minimal.
9. SOFTWARE DESIGN COST
   - Proportional to the thoroughness of the tests required.
10. WEIGHT
    - Weight increases as the number of memory chips required increases.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST	
CATEGORY: LONG TUTORIAL	**PAGE** 8 **of** 12
SUBCATEGORY: DEFAULT DESIGN	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

a) SEE FIGURE 3 FOR MICROPROCESSOR BIT LEVEL II BLOCK DIAGRAM

b) SEE FIGURE 4 FOR MICROPROCESSOR BIT DEFAULT DESIGN

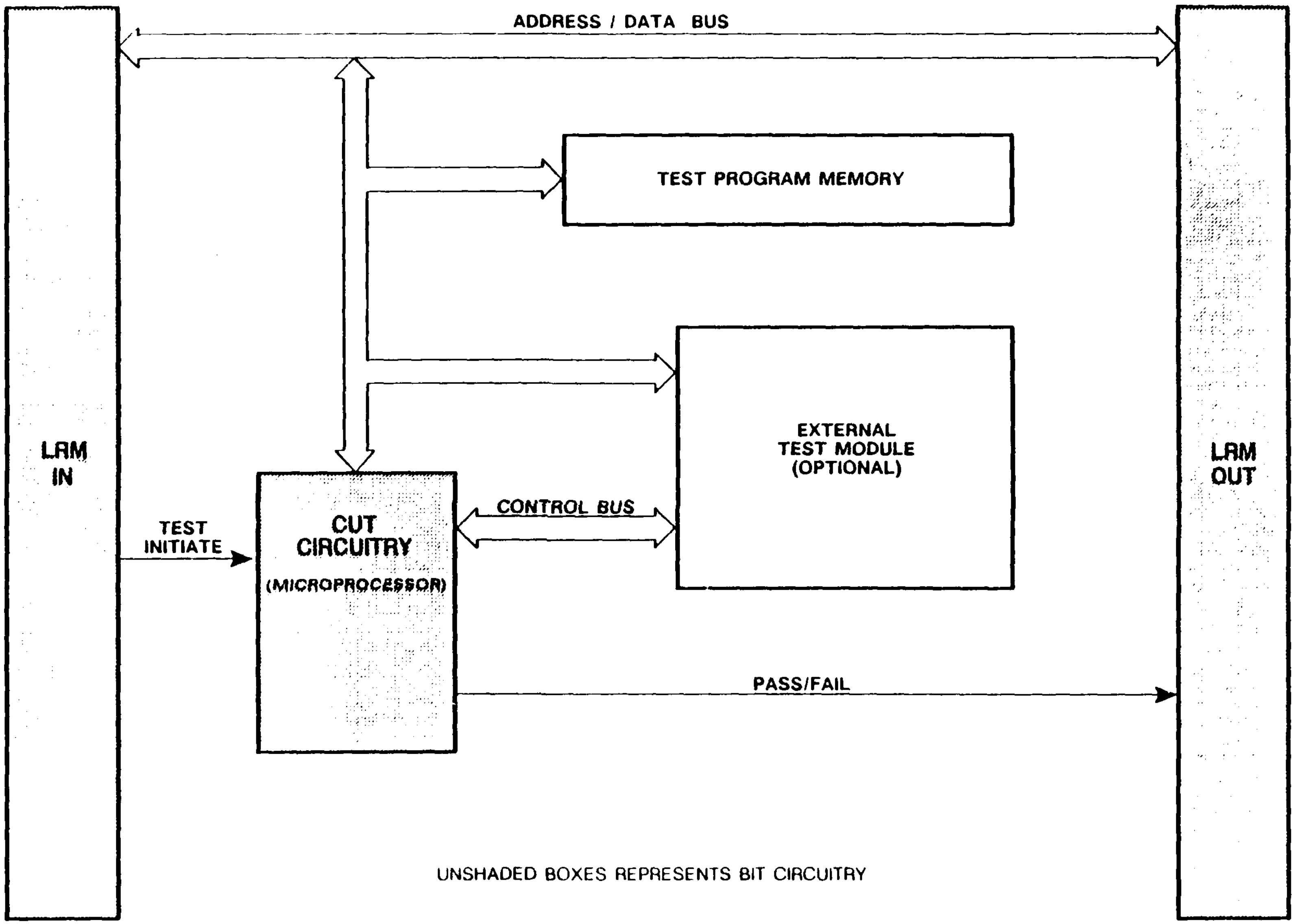


FIGURE 3 LEVEL II BLOCK DIAGRAM
MICROPROCESSOR BIT

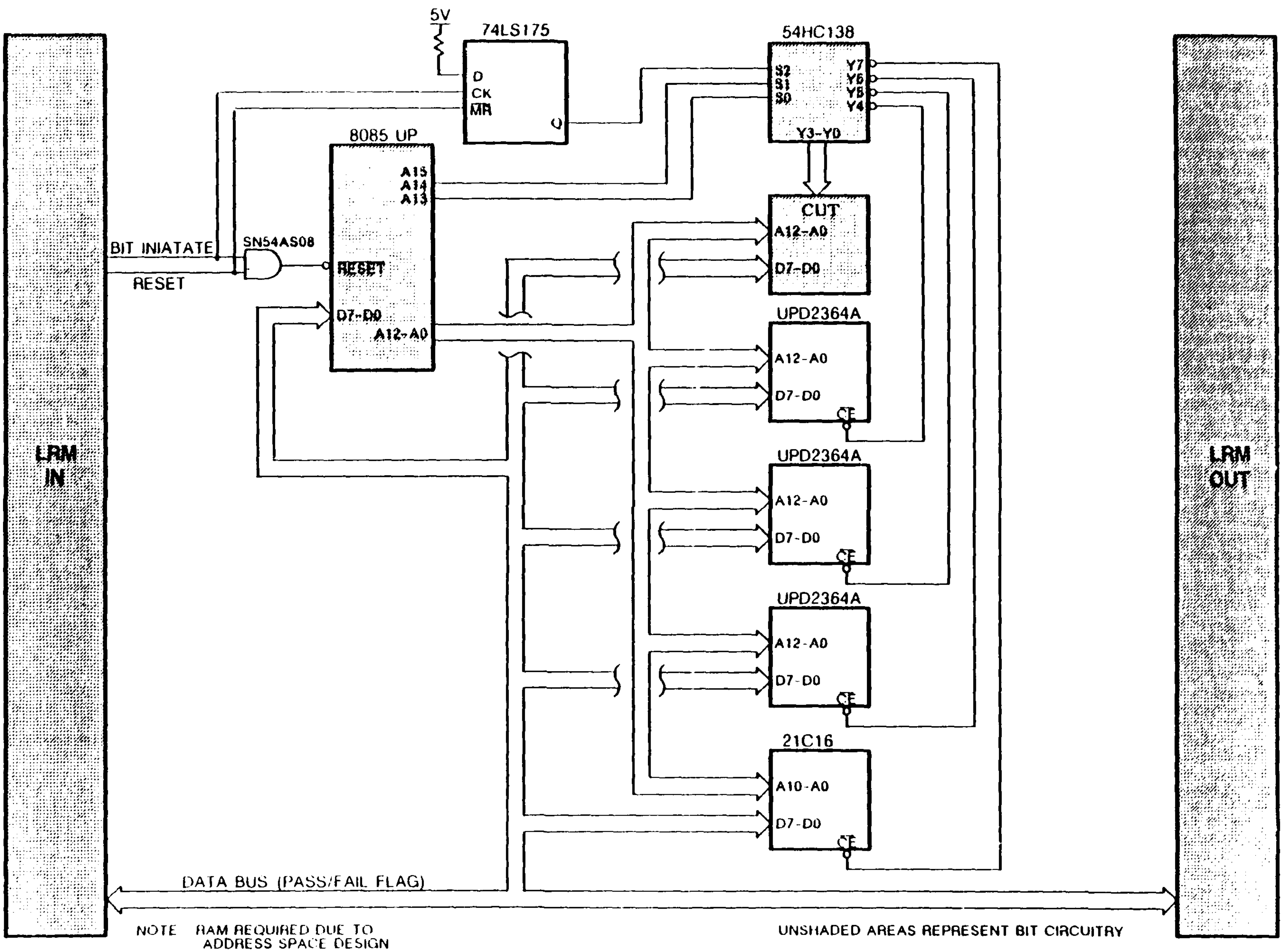


FIGURE 4 DEFAULT DESIGN (MICROPROCESSOR BIT)

PAGE 10 of 12

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: LONG TUTORIAL

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

MICROPROCESSOR BUILT-IN-TEST
PARTS DATA TABLE

NUMBER/NAME	AREA *(sq in)*	# OF PINS	POWER TYPICAL *(mW)*	POWER MAX. *(mW)*	WEIGHT *(grns)*
74LS175/ D FLIP FLOP	0.20	16	60	90	0.9
SN54AS08/ AND CHIP	.24	14	260	440	1.1
uPD2364A/ 8K ROM	.78	24	200	350	3.5
21C16/ 2K RAM	.21	24	10	19	0.95

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST	
CATEGORY: LONG TUTORIAL	PAGE 12 of 12
SUBCATEGORY: BIBLIOGRAPHY	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

NONE REQUIRED

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: USER REQUESTED DATA

SUBCATEGORY:

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

QUESTIONS	VARIABLE ASSIGNMENT
1. What is the total amount of test memory required in Kbytes?	v1
2. What is the operation speed of the microprocessor in Kbytes/sec?	v2

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITION

$n1$ = Number of Flip Flop chips

$n2$ = Number of AND chips

$n3$ = Number of ROM memory chips

$n4$ = Number of RAM chips

$v1$ = Total number of bytes in the test program (Kbytes)

$v2$ = Operating speed of the microprocessor (Kbytes/sec)

II) COMPONENT DETERMINATION EQUATIONS

$n1 = 1$

$n2 = 1$

$n3 = v1/8$

$n4 = 1$

III) PENALTY EQUATIONS

a) AREA (sq in)

$$\text{Area of BIT chips} = (.20)n1 + (.24)n2 + (.78)n3 + (.21)n4$$
$$= .65 + (.78)n3$$

$$\text{Total area of BIT circuitry} = (\text{Area of BIT chips}) + 15\% \text{ for PC traces}$$
$$= 1.15\ (\text{Area of BIT chips})$$

b) WEIGHT (gms)

$$\text{Weight of BIT chips} = (.90)n1 + (1.1)n2 + (3.5)n3 + (.95)n4$$
$$= 2.95 + (3.5)n3$$

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICROPROCESSOR BUILT-IN-TEST

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: **TEXT** ☐ **LIST** ☐ **TABLE** ☐ **GRAPHIC** ☐ **EQUATIONS** ☒

DATA:

b) WEIGHT (CONT)

Total weight of BIT circuitry = (Weight of BIT chips) + 10% For weight of solder
= 1.1 (Weight of BIT chips)

II) PENALTY EQUATIONS (CONT)

c) POWER (mW)

Total power consumption of BIT chips = $(60)n1 + (260)n2 + (200)n3 + (10)n4 = 330 + (200)n3$

d) TEST TIME

Total time for microprocessor BIT = $v1/v2$

PARAGRAPH 6.3
MICRODIAGNOSTICS TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS

CATEGORY: SHORT TUTORIAL	**PAGE** 1 **of** 4

SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE

DATA TYPE: **TEXT** [x] **LIST** [ ] **TABLE** [ ] **GRAPHIC** [ ] **EQUATIONS** [ ]

DATA:

SHORT TUTORIAL FOR MICRODIAGNOSTICS BIT TECHNIQUE

Microdiagnostics is a diagnostic bit technique that is implemented by microprogramming on a microcode level. It has been shown that by implementing a Built-In-Test (BIT) test on the microcode level in a microprogramming environment, hardware/software utilization is optimized. This solution eliminates the need for a hardware intensive approach compared to a microcode level BIT running out of firmware or secondary storage.

The technique involves partitioning an area of the "micro-program-store" to support a small BIT routine, which would be executed by a macro instruction that could be called RUNBIT. When the OPCODE for RUNBIT is encountered in an external program, the specified address of the BIT routine would be vectored to.

This micro-coded BIT would verify operation of the processor circuitry by testing all its elements. The register stack and all internal Random Access Memory (RAM) can be exhaustively checked. A checksum can be generated for micro-program store and compared with a previously stored value. All Arithmetic & Logic Unit (ALU) functions can be checked along with the associated flags and status bits. Data can be routed along all points of the internal buses to verify operation of the multiplexing circuitry. This BIT could either be run as a subroutine, that is, all status and contents of registers placed on stack before execution and restored after BIT is completed, or it could be a stand alone procedure which initializes the processor after completion.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS	
CATEGORY: SHORT TUTORIAL	**PAGE** 2 **of** 4
SUBCATEGORY: 1. LEVEL I BLOCK DIAGRAM 2. BIT SEQUENCE FLOW CHART	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2

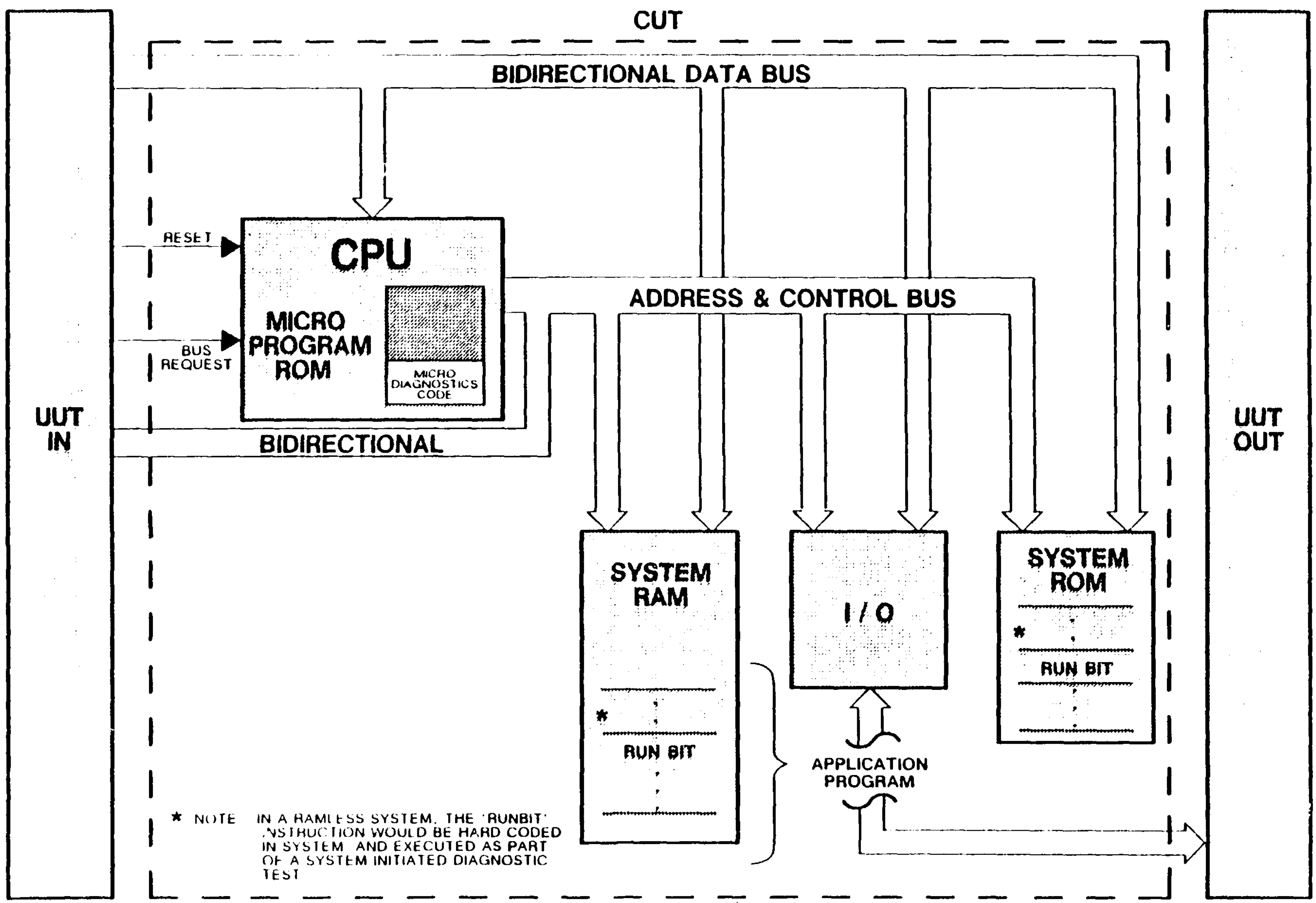


FIGURE 1 LEVEL I BLOCK DIAGRAM MICRODIAGNOSTICS

PAGE 3 of 4

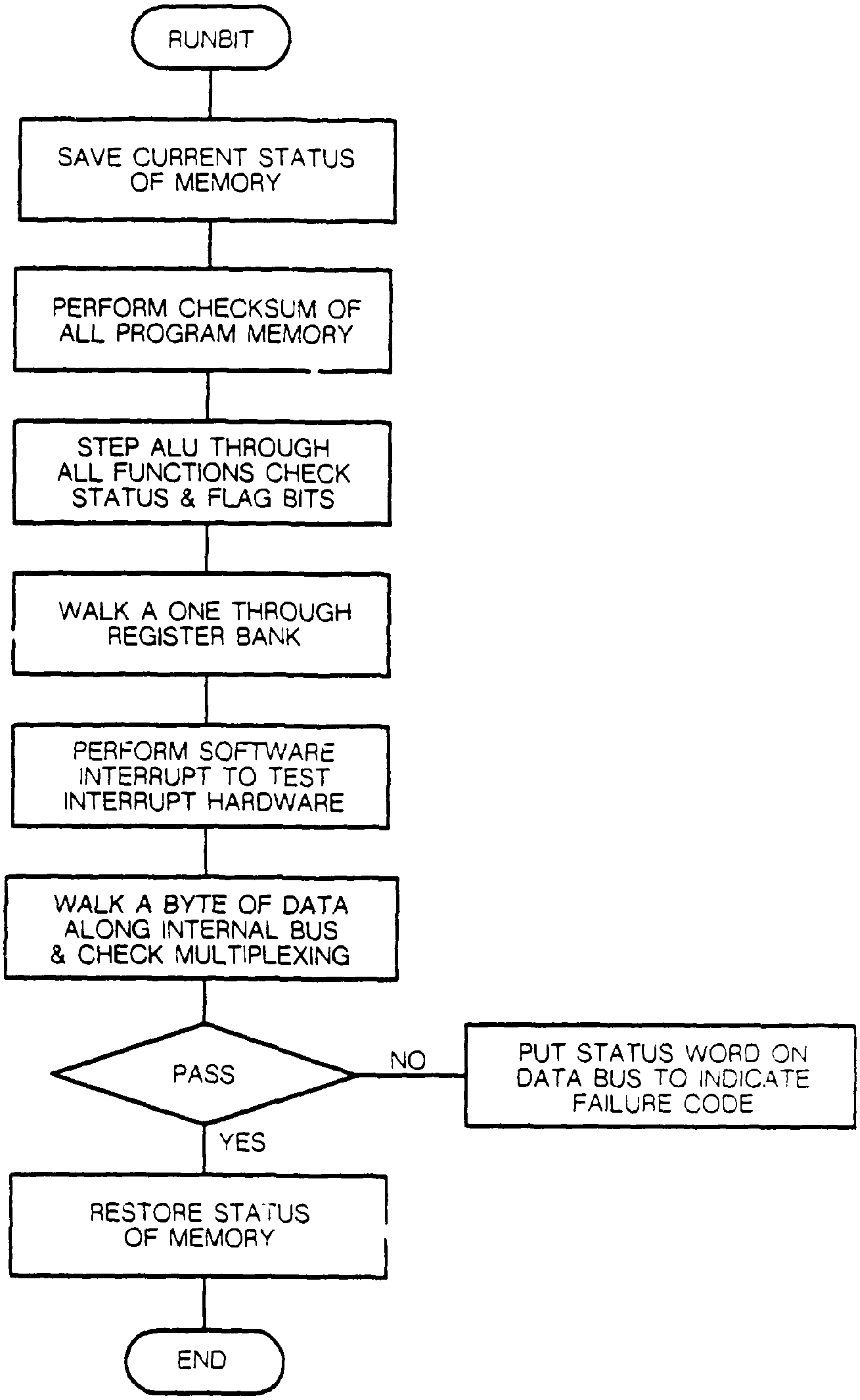


FIGURE 2 BIT SEQUENCE FLOW CHART FOR MICRODIAGNOSTICS

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS

CATEGORY: LONG TUTORIAL | **PAGE** 1 **of** 11

SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
MICRODIAGNOSTICS BIT TECHNIQUE

1. Macro instruction "RUNBIT" is called to initiate testing.

   - Perform checksum of all program memory.
   - Step "ALU" through all functions. Check status and flag bits.
   - Walk a one through register banks.
   - Perform software interrupt test.
   - Walk various data patterns along internal bus and check system multiplexing paths.

2. If all tests pass, restore status of memory and registers to the original status before RUNBIT was called.

3. If test fails, put known status word on data bus to indicate failure code. This result can be output from Line Replaceable Module (LRM) to rest of system.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

MICRODIAGNOSTICS BIT TECHNIQUE ADVANTAGES

1. No software overhead due to microcode "RUNBIT" program.

2. Because the BIT is on a microcode level, BIT will run at a fast rate.

3. Provides quick confidence level because of fast BIT.

4. Can check internal microcomputer circuitry, as well as peripheral chip functions.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE DISADVANTAGES

DATA TYPE: TEXT [ ] LIST [x] TABLE [ ] GRAPHIC [ ] EQUATIONS [ ]

DATA:

MICRODIAGNOSTICS BIT TECHNIQUE
DISADVANTAGES

1. Possible large hardware requirements due to size of microcode program memory needed to handle BIT test. Example: Large BIT slice configurations with limited memory.

2. Because BIT is constrained to micro program memory it will have to be small in nature and may not check all of the BIT slice configuration.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS	
CATEGORY: LONG TUTORIAL	**PAGE** 4 **of** 11
SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

MICRODIAGNOSTICS BIT TECHNIQUE ATTRIBUTES

1. REAL ESTATE PENALTY -
   - None, as long as memory is available for BIT test.
   - If memory not available, Read Only Memorys (ROMs) should be added proportional to microcode program and extent of peripheral circuitry.
2. POWER PENALTY -
   - Roughly proportional to real estate penalty example:
     Power Penalty = % Real Estate Penalty X Circuit Under Test (CUT) Normal Power
   - Execution - Some ROMs have power down mode
   - Switch technology - Use Metal Oxide Semiconductor (MOS) ROMs for higher density
3. RELIABILITY PENALTY -
   - Proportional to Real Estate Penalty, if similar technology is used for Built-In Test Equipment (BITE) as for CUT.
4. TIMING PENALTY -
   - Test Time Duration - Number of BIT instructions multiplied by the average execution time of instructions.
5. NON-CONCURRENT
6. CONCEPTUAL COMPLEXITY - Straight forward

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

MICRODIAGNOSTICS BIT TECHNIQUE ATTRIBUTES

7. HARDWARE/SOFTWARE/COMBO - HARDWARE
   - Test patterns or instruction code in firmware
8. TECHNOLOGY -
   - All current digital technologies
   - May use higher density technologies for ROM to reduce any extra real estate penalty.
9. IS BITE SELF TESTABLE -
   - Can do checksum on all memory including BIT.
   - Can use serial shadow resistors diagnostic registers to monitor BIT
10. DESIGN COST -
    - Minimal due to microcode and no hardware design.
11. FIRMWARE DESIGN COST -
    - Dependent on microcode complexity.
12. NUMBER OF BYTES OF STORAGE REQUIRED -
    - Function of complexity of CUT and memory and number of peripheral devices.
13. STAND ALONE (SELF CONTAINED BIT)?
    - Yes (in ROM memory microcode).

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

MICRODIAGNOSTICS BIT TECHNIQUE ATTRIBUTES

14. WEIGHT -
    * Proportional to real estate penalty.
15. COMMERCIALLY AVAILABLE INTEGRATED CIRCUITS WITH TESTABILITY FEATURES -
    * ROMs available with shadow registers.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS	
CATEGORY: LONG TUTORIAL	**PAGE** 7 **of** 11
SUBCATEGORY: DEFAULT DESIGN	

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐

DATA:

a) SEE FIGURE 3 FOR MICRODIAGNOSTICS BIT LEVEL II BLOCK DIAGRAM

b) SEE FIGURE 4 FOR MICRODIAGNOSTICS BIT DEFAULT DESIGN

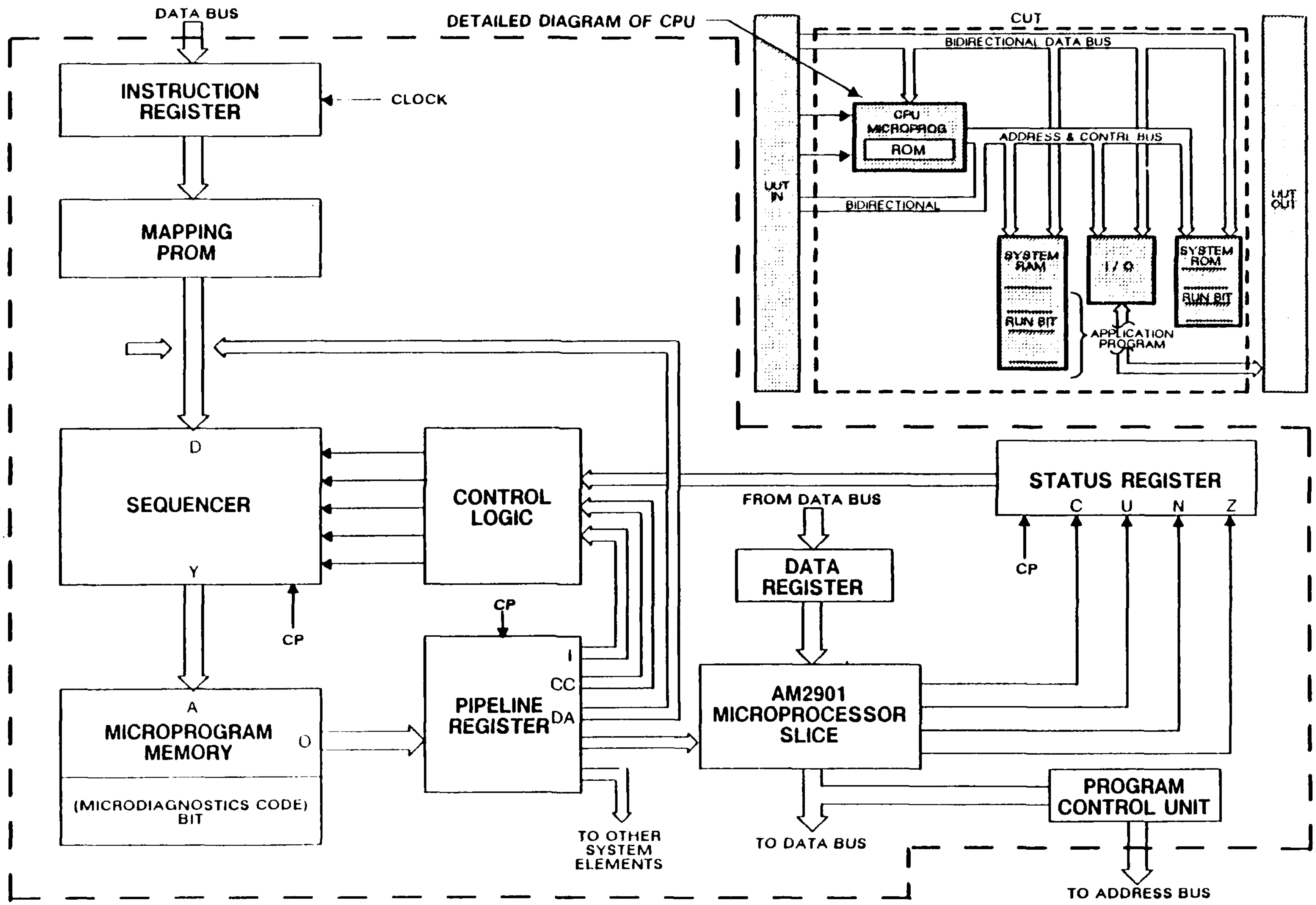
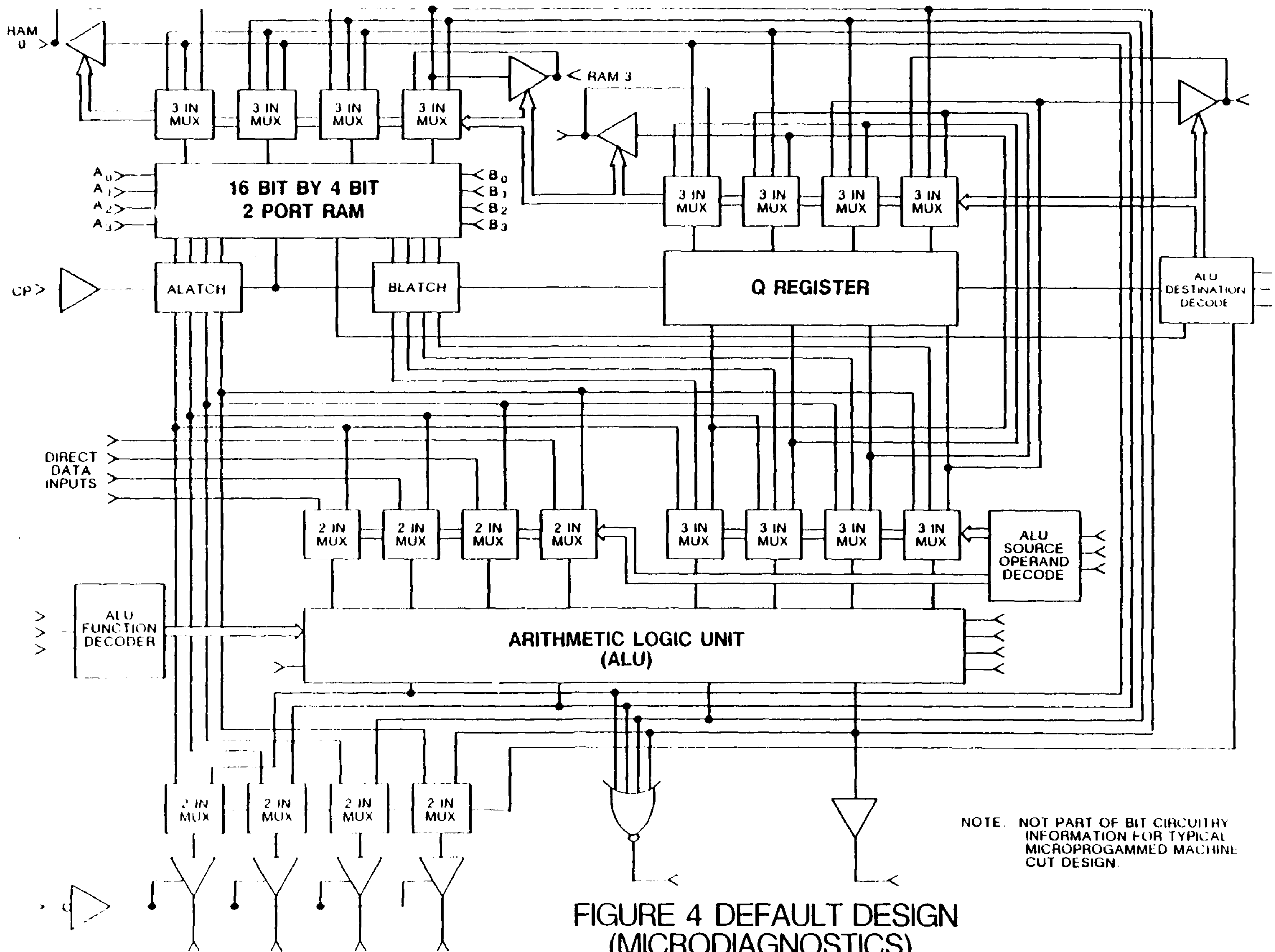


FIGURE 3 LEVEL II BLOCK DIAGRAM MICRODIAGNOSTICS



NOTE. NOT PART OF BIT CIRCUITRY INFORMATION FOR TYPICAL MICROPROGAMMED MACHINE CUT DESIGN.

FIGURE 4 DEFAULT DESIGN (MICRODIAGNOSTICS)

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS

CATEGORY: LONG TUTORIAL

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

NUMBER/NAME	AREA *(sq in)*	# OF PINS	POWER TYPICAL*(mW)*	POWER MAX. *(mW)*	WEIGHT *(gms)*
MM5220 ROM	0.375	24	150	325	N/A

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIBLIOGRAPHY

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

1. T. Sridhar and J.P. Hayes, "Testing bit-sliced microprocessors" in Proc. 9th Int. Conf. Fault-Tolerant Computing. Madison, WI: IEEE Comp. Soc. June 1979 PP 211-218.

2. The AM2900 Family Databook, Advanced Micro Devices, Sunnyvale, CA., 1976.

3. D.P. Fulghum, "Automatic Self-Test of a Microprocessor System", Proc. Autotestcon 1976, Arlington, Texas, Nov. 1976. PP 47-52 (Abstracts in IEEE Trans, Aerospace and Electronic Systems, Vol. AES-13 No. 2, March 1977).

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS

CATEGORY: USER REQUESTED DATA

SUBCATEGORY:

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

QUESTIONS	VARIABLE ASSIGNMENTS
1. How many microcode BIT lines are used by the CPU?	v1
2. How many BIT Instruction words are required to be stored in the additional ROMs?	v2
3. What is the test pattern application rate?	v3
4. What is the estimated initialization time?	v4

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: **TEXT** ☐ **LIST** ☐ **TABLE** ☐ **GRAPHIC** ☐ **EQUATIONS** ☒

DATA:

I) VARIABLE DEFINITION

n1 = Number of ROM chips

v1 = Number of microcode BIT data lines used by the CPU

v2 = Number of BIT instruction words to be stored in additional ROMs

v3 = BIT instruction execution rate

v4 = Estimated initialization time

II) COMPONENT DETERMINATION EQUATIONS

$n1 = (v1/8)(v2/2048)$

$v1 <= 120$

$v2 <= 6144$

III) PENALTY EQUATIONS

a) AREA (sq in)

Total area of BIT chips = (0.375)n1

Total area of BIT circuitry = (Total area of BIT chips) + 15% FOR PC traces
= 1.15 (total area of BIT chips)

b) WEIGHT (gms)

Weight of BIT chips = (6.5)n1

Weight of BIT circuitry = Weight of BIT chips + 10% For weight of solder = 1.1 (Weight of chips)

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: MICRODIAGNOSTICS	
CATEGORY: EQUATIONS	**PAGE** 2 **of** 2
SUBCATEGORY: (DATA NOT TO BE DISPLAYED)	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒	

DATA:

c) POWER (mW)

MAX POWER = (325)n1

III) PENALTY EQUATIONS

d) TEST TIME

TEST TIME = (v2)(v3) + v4

PARAGRAPH 6.4

ON-BOARD INTEGRATION OF VLSI CHIP BIT (OBIVCB) TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT

CATEGORY: SHORT TUTORIAL

SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE

DATA TYPE: TEXT [X] LIST [ ] TABLE [ ] GRAPHIC [ ] EQUATIONS [ ]

DATA:

SHORT TUTORIAL
FOR
ON-BOARD INTEGRATION OF VLSI CHIP BIT (OBIVCB)

OBIVCB is a technique which makes extensive use of Built-In-Self-Test (BIST) internal to integrated circuits resident on the circuit board. It does this by providing a "Processor Test Node" on the board, which is capable of addressing a variety of chip Built-In-Test (BIT) approaches. For instance, the processor node will be capable of supplying pseudo-random test patterns and collecting signatures for the integrated circuits which contain internal scan circuitry. It will also be capable of initiating and regulating self-test on chips that contain a BIST. Additionally, it will be capable of testing chips which contain no BIST circuitry by running a conventional BIT stored in Processor Node firmware.

In general, the Processor Node will coordinate chip self-testing, allowing for parallel testing, and taking advantage of the more current techniques of self-test.

Types of BIT supported by OBIVCB:

- Scan path techniques
- Internally supported scan, boundary scan Test and Measurement (TM) bus. i.e. pseudo-random pattern generation and signature analysis is provided on chip.
- Visibility block approach: Built In Logic Block Observer (BILBO), shadow registers, configurable test points etc...
- Conventional BIST with chip fail or status flags.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT	
CATEGORY: SHORT TUTORIAL	**PAGE** 2 **of** 5
SUBCATEGORY: 1. LEVEL I BLOCK DIAGRAM 2. BIT SEQUENCE FLOW CHART	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2

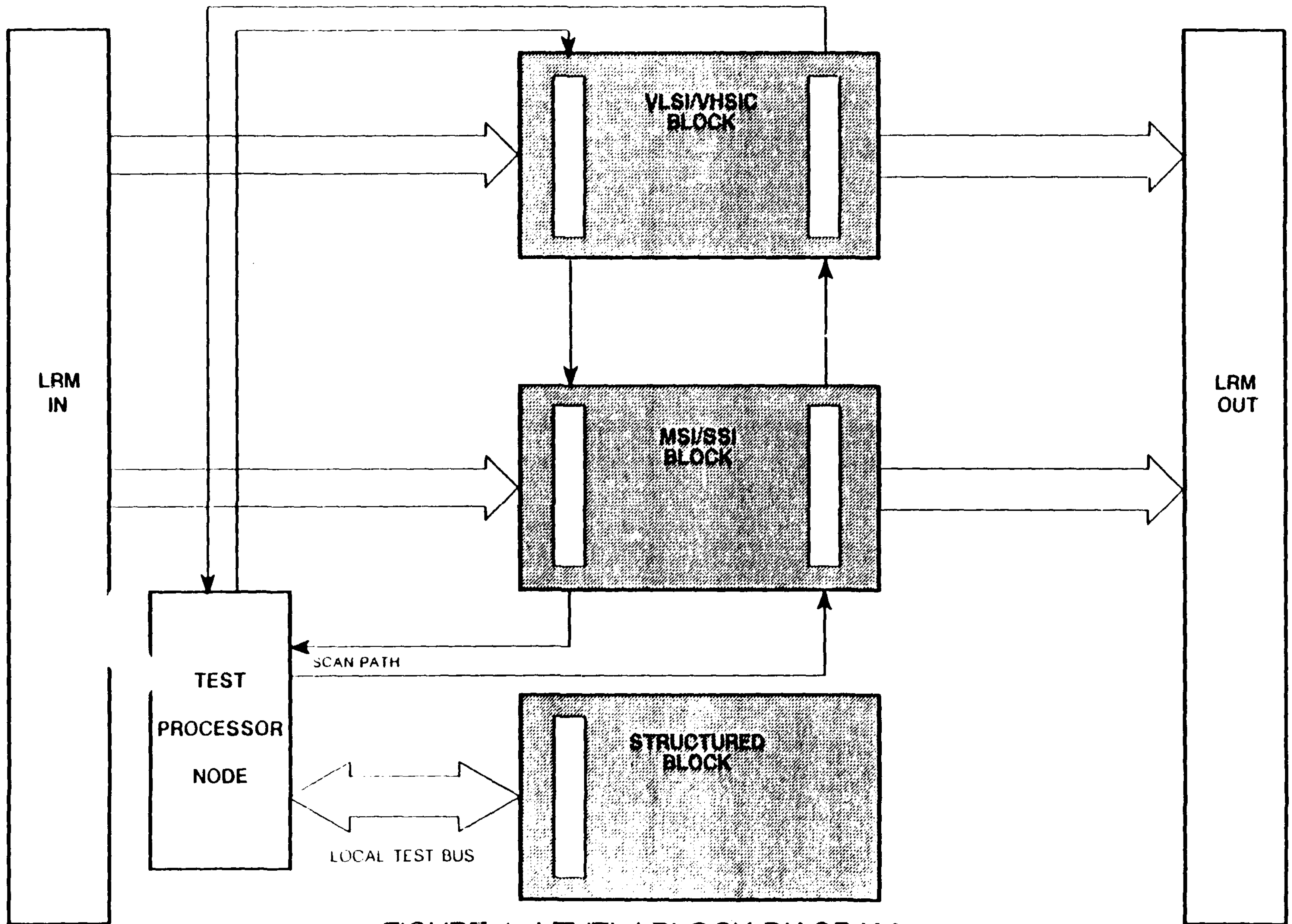


FIGURE 1 LEVEL I BLOCK DIAGRAM
ON-BOARD INTEGRATION of VLSI CHIP BIT

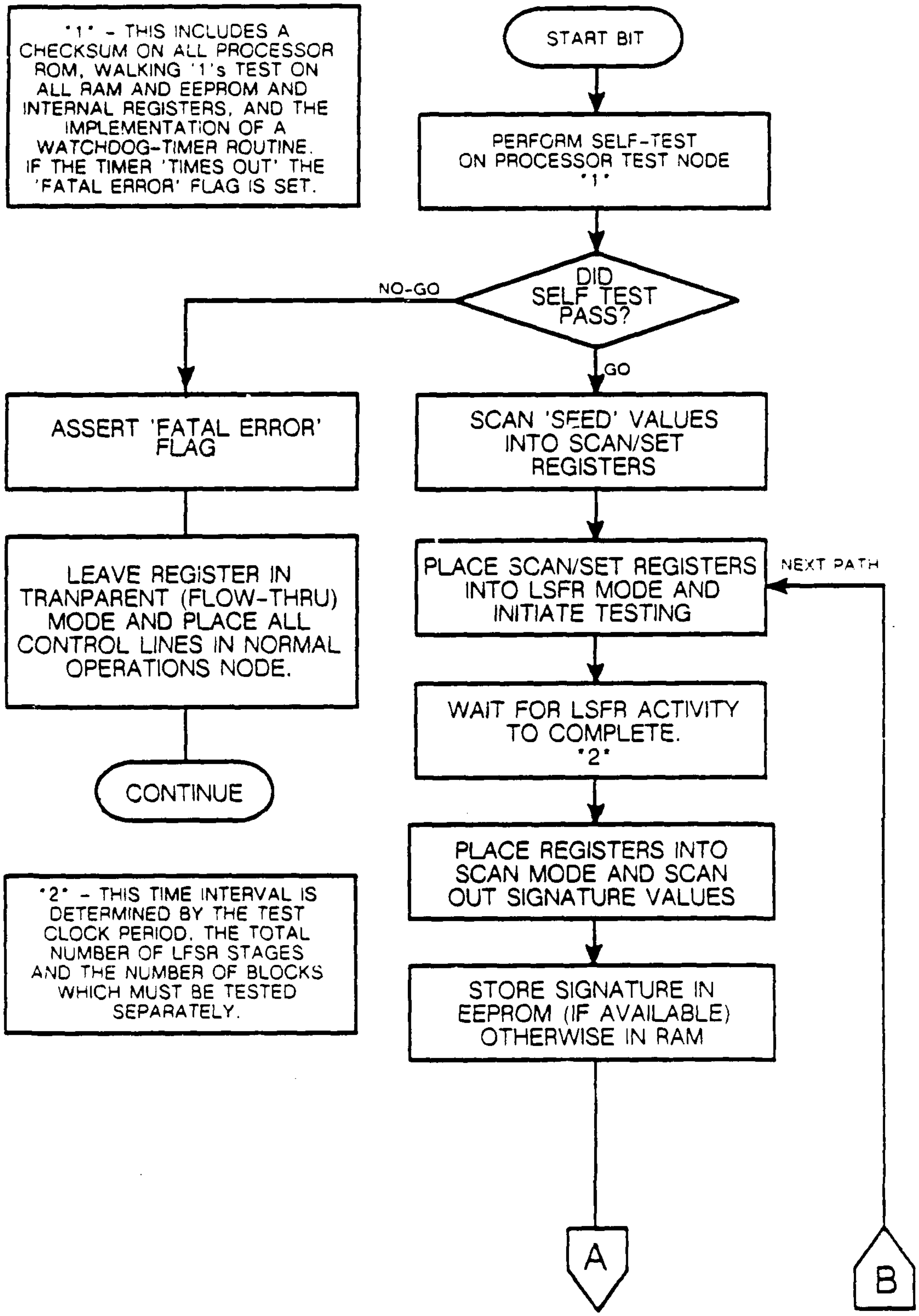


FIGURE 2 BIT SEQUENCE FLOW CHART FOR OBIVCB

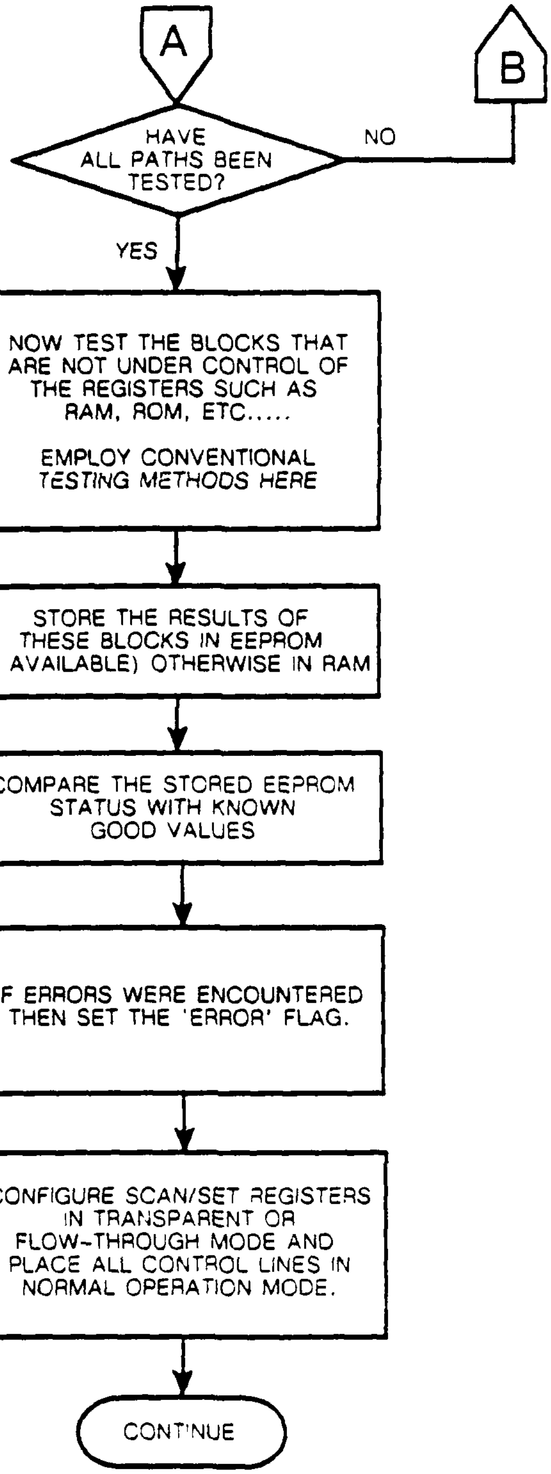


FIGURE 2 (CONT) BIT SEQUENCE FLOW CHART FOR OBIVCB

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
ON-BOARD INTEGRATION OF VLSI CHIP BIT (OBIVCB)

1. BIT is initiated either upon power-up or externally by a pulse. A reset pulse is sent to all chips which can be initialized, as well as the processor which vectors it to a self test procedure.

2. The Test Processing Node performs a self test. This includes a complete test of read/write memory as well as checksum tests on all program memory. All registers are tested and a "watch-dog" timer routine is implemented.

3. Upon successful completion of (2), the processor reads a configuration block in memory which tells it such things as:

   - which and how many Scan/Set (S/S) registers need to be initialized.
   - which test loops should be assigned to which registers.
   - place S/S register in pattern generation, signature, or scan mode, for example.
   - which loops can be run concurrently.
   - which "seeds" to place in S/S registers.

4. Scan seed values into S/S registers, set loop sequencer multiplexer, and send signal to execute chip BITs.

5. When this wave of testing is completed (either by establishing pseudo-random pattern length or by waiting for external chips handshake signal) configure S/S registers in serial scan mode and scan values into the processor node. Results may be stored in Electrically Erasable/Programmable Read Only Memory (EEPROM) if one is used.

6. If there are chips that need to be tested separately then repeat steps (4) and (5) until all scannable integrated circuits are accounted for.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT	
CATEGORY: LONG TUTORIAL	**PAGE** 2 **of** 13
SUBCATEGORY: TEST SEQUENCE DESCRIPTION	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
ON-BOARD INTEGRATION OF VLSI CHIP BIT (OBIVCB)
(CONT)

7. Now, if there are blocks which require conventional testing, branch to the area where BIT firmware resides in Test Node program memory and perform this BIT by exercising stimulus and response vectors via the test bus.

8. Examine the results of all testing as stored in EEPROM and if errors exist set ERROR flag.

9. Send signal to circuit under test to initiate or resume normal operation and tristate all Test Processor Node buses.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ON-BOARD INTEGRATION OF VLSI CHIP BIT
ADVANTAGES

1. In defining a Test Processor Node architecture, a standard hardware interface is achieved which can be used for widely varying chip BITs. This standard can later be put into a gate array or standard cell, making implementation as simple as designing in a single chip.

2. Because a dedicated processor is used, it is extensible and easily modified by rewriting firmware.

3. In making extensive use of scan path, pseudo-random pattern generation, and signature analysis, minimum analysis is required from the designer as this is a hardware, rather than software, driven test.

4. Linear Feedback Shift Register (LFSR) theory, the basis of pattern generation signature analysis, is well established and documented. Its exhaustive level of fault detection has been the subject of several papers.

5. In tying together various chip BITs with a single Processor Node, a hierarchical test structure is built which is well defined and maintainable. This idea can be extended from the card to the box and system levels.

6. Also for the above reason, a hardware / software balance is achieved, allowing time costs and chip costs to be worked into project budgets more easily than an approach which is radically hardware or software intensive.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT SEQUENCE DISADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ON-BOARD INTEGRATION OF VLSI CHIP BIT (OBIVCB) DISADVANTAGES

1. This approach requires the circuit under test to be largely self testing; that is, it assumes that BIT is included in most of the chips, especially the Very Large Scale Integration (VLSI) and Very High Speed Integrated Circuits (VHSIC) devices.

2. A Processor Test Node is required, while not comprising an unreasonable amount of hardware for testing a board of complex logic, may be over kill if the logic is accessible and not particularly complex. Each application has to be evaluated separately on the basis of need.

3. The test hardware has been optimized for scan path type testing. While it can handle other approaches as well, it tends to constrain circuit design, both on the board level as well as the chip level, to this type of structure.

4. Including testability on chip, by providing test cells in Application Specific Integration Circuits (ASICs), the effective level of on-chip integration drops. Note that in designing gate arrays, routing becomes progressively more difficult as more of the gates are utilized. For this reason delays can be introduced in the chip.

5. With the growing popularity of ASICs, the boundary between board level design and chip level design is becoming fuzzy. OBIVCB calls for a level of cooperation between conventional board level designers and silicon design. Currently, Design For Test (DFT) on the chip level is not widely implemented.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT

CATEGORY: LONG TUTORIAL | **PAGE** 5 **of** 13

SUBCATEGORY: BIT SEQUENCE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ON-BOARD INTEGRATION OF VLSI CHIP BIT (OBIVCB) ATTRIBUTES

1. REAL ESTATE PENALTY -

   - Defined by base configuration (four test loops and eight parallel test lines). There is a small initial jump as configuration expands beyond the base and increases linearly with serial and parallel growth. Control lines increases as the log of the number of test loops. Actual area is given for Dual-In-Line Packages (DIPs) and can be reduced if modem packaging techniques are employed; i.e. Small Outline Packages, Pin Grid Arrays, and Plastic Leaded Chip Carriers.

2. POWER PENALTY -

   - Roughly linear with expansion and very dependent on technology used. For instance, if Complementary Metal Oxide Semiconductor (CMOS) implementations are employed the power savings are the greatest.

3. RELIABILITY PENALTY -

   - More dependent on the number of packages than on equivalent number of gates. This suggests using as highly integrated circuits as possible.

4. TIMING PENALTY -

   - Timing is divided into two groups:
   - Serial testing - grows exponentially with LFSR length and is a product of scanning frequency.
   - Parallel test - via a BIT stored in controller Read Only Memory (ROM). Proportional to the complexity of the Circuit Under Test (CUT) to be tested by the parallel bus. Expansion of the Parallel lines should have no effect on test time.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT

CATEGORY: LONG TUTORIAL | **PAGE** 6 of 13

SUBCATEGORY: BIT SEQUENCE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ON-BOARD INTEGRATION OF VLSI CHIP BIT (OBIVCB)
ATTRIBUTES
(CONT)

5. CONCURRENCY -

   This approach is non concurrent.

6. CONCEPTUAL COMPLEXITY - Embodies two ideas:

   - Embedded controller with standard BIT stored in firmware.
   - Linear Feedback Shift Register theory and its attendant scan-path testing schemes.

   While both these approaches have been well established in the test industry, the idea of combining them in this particular way has not.

7. HARDWARE/SOFTWARE TRADEOFF -

   - LFSRs require only initial 'seed' values, and the capability of scanning signatures into the processor. This minimizes software and makes use of a highly compact hardware algorithm.

8. TECHNOLOGY -

   - This design lends itself to a technology with a good power/integration product. CMOS III is an example of a good process for this.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT	
CATEGORY: LONG TUTORIAL	PAGE 7 of 13
SUBCATEGORY: DEFAULT DESIGN	

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐

DATA:

a) SEE FIGURE 3 FOR ON-BOARD INTEGRATION OF VLSI CHIP BIT LEVEL II BLOCK DIAGRAM - TEST PROCESSOR NODE

b) SEE FIGURE 4 FOR ON-BOARD INTEGRATION OF VLSI CHIP BIT LEVEL III WIRING DIAGRAM - TEST PROCESSOR NODE

c) SEE FIGURE 5 FOR ON-BOARD INTEGRATION OF VLSI CHIP BIT LEVEL III WIRING DIAGRAM - TEST PROCESSOR NODE (CONT)

d) SEE FIGURE 6 FOR ON-BOARD INTEGRATION OF VLSI CHIP BIT LEVEL III WIRING DIAGRAM - 1 OF 4 SCAN/SET REGISTERS - DETAIL

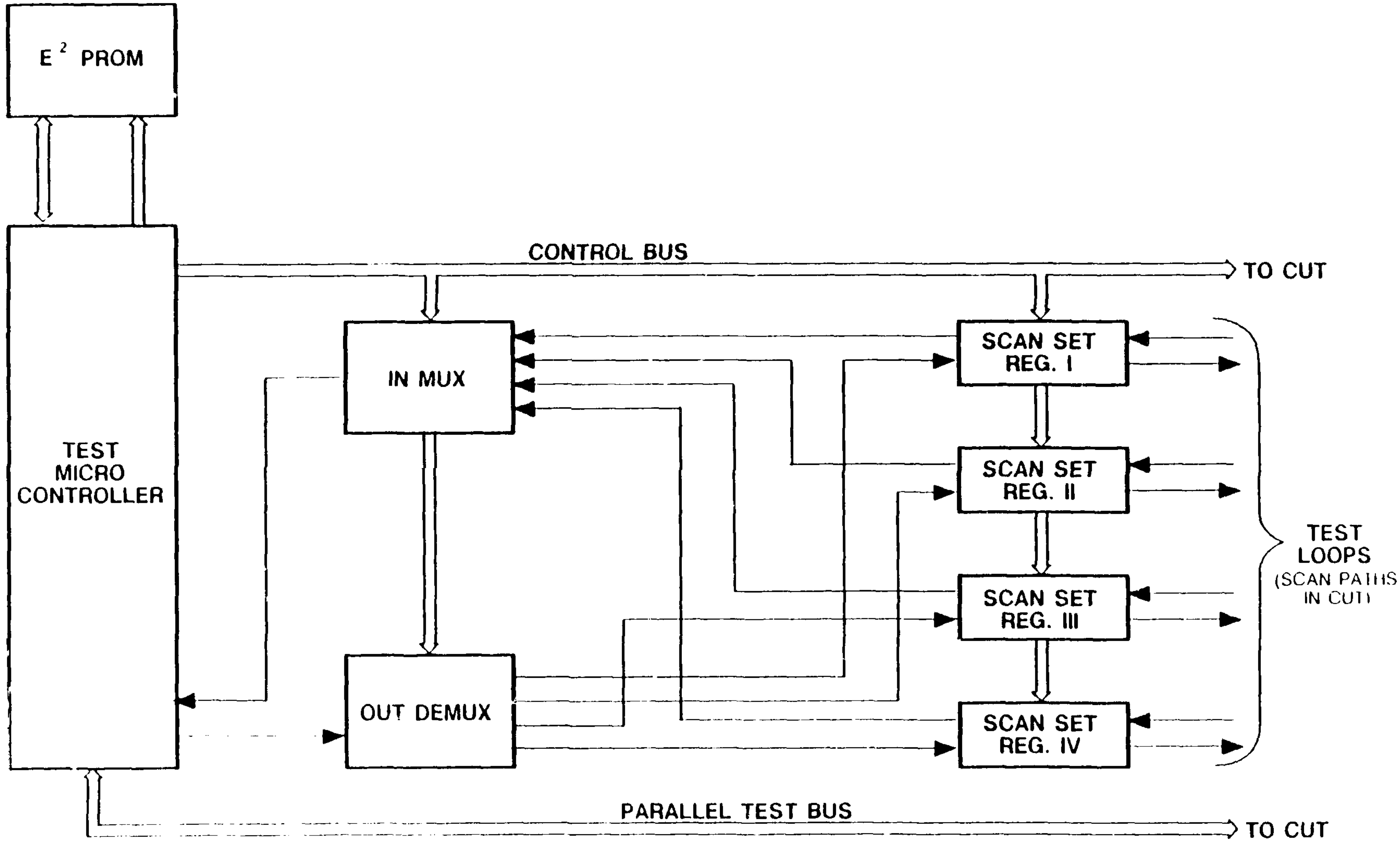
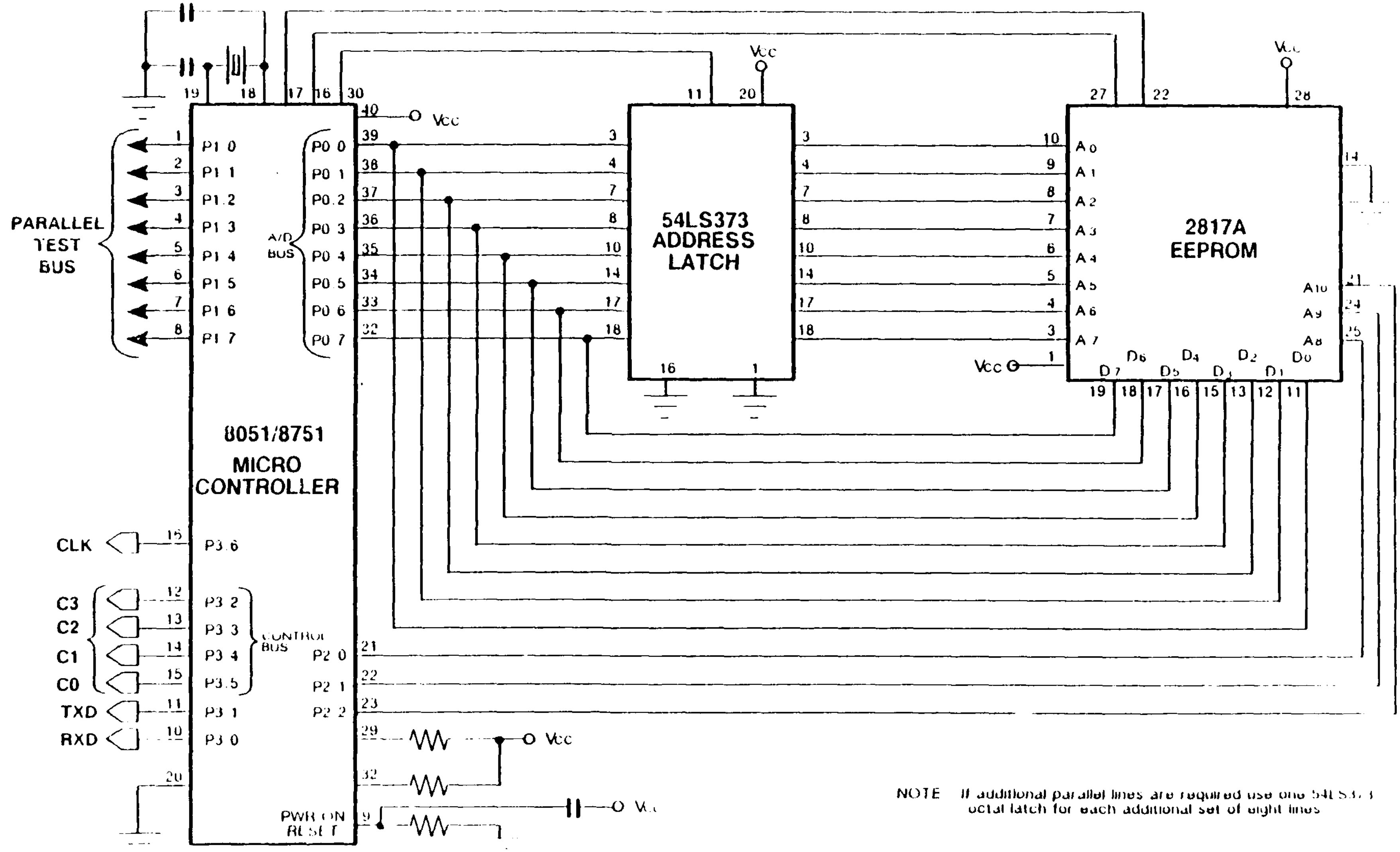


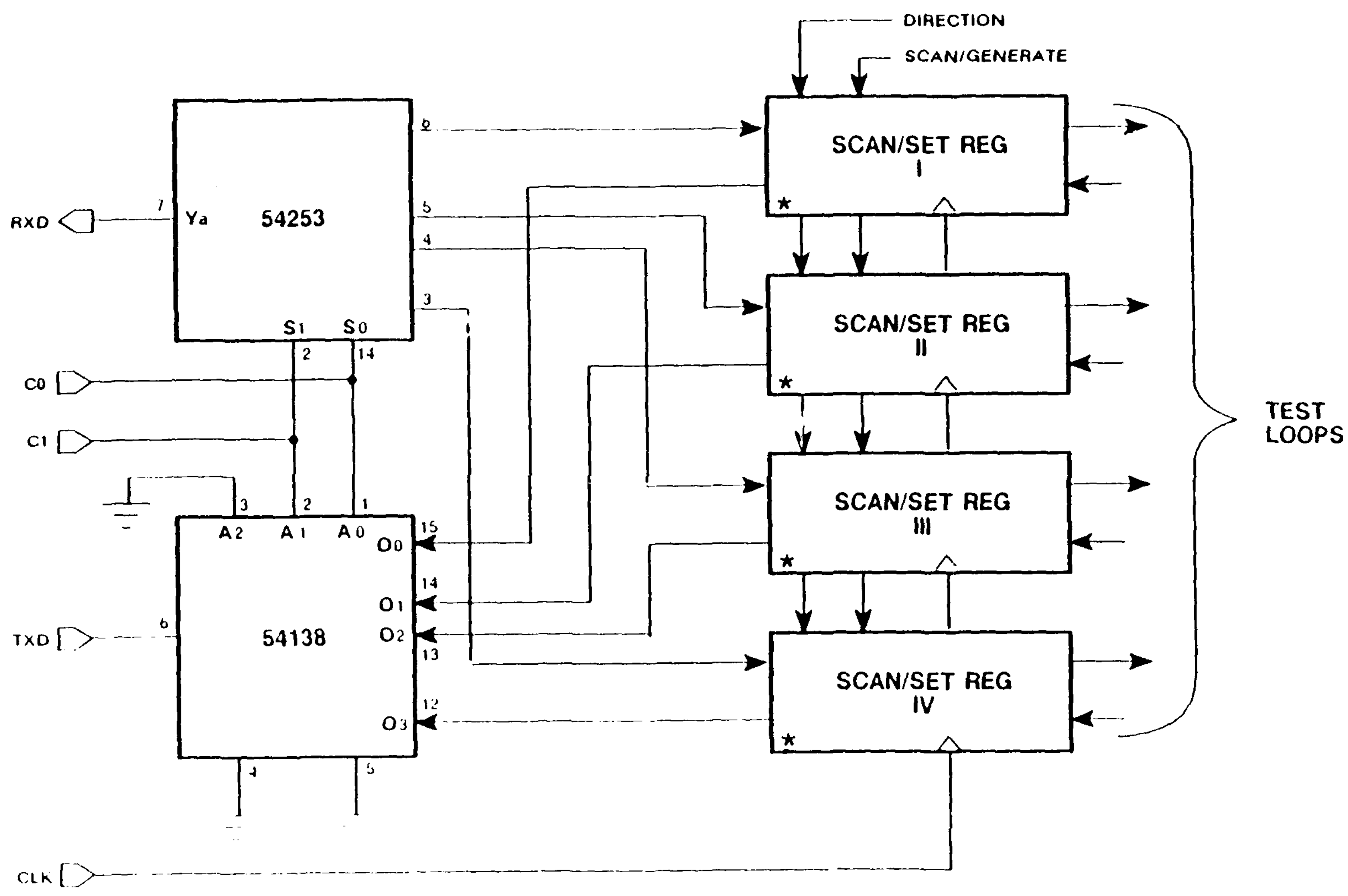
FIGURE 3 LEVEL II BLOCK DIAGRAM
TEST PROCESSOR NODE



NOTE If additional parallel lines are required use one 54LS373 octal latch for each additional set of eight lines

FIGURE 4 LEVEL III WIRING DIAGRAM
TEST PROCESSOR NODE

OBIVCB



★ FOR DETAIL OF SCAN SET REG SEE FIGURE 6

FIGURE 5 LEVEL III WIRING DIAGRAM TEST PROCESSOR NODE (CONT)

OBIVCB

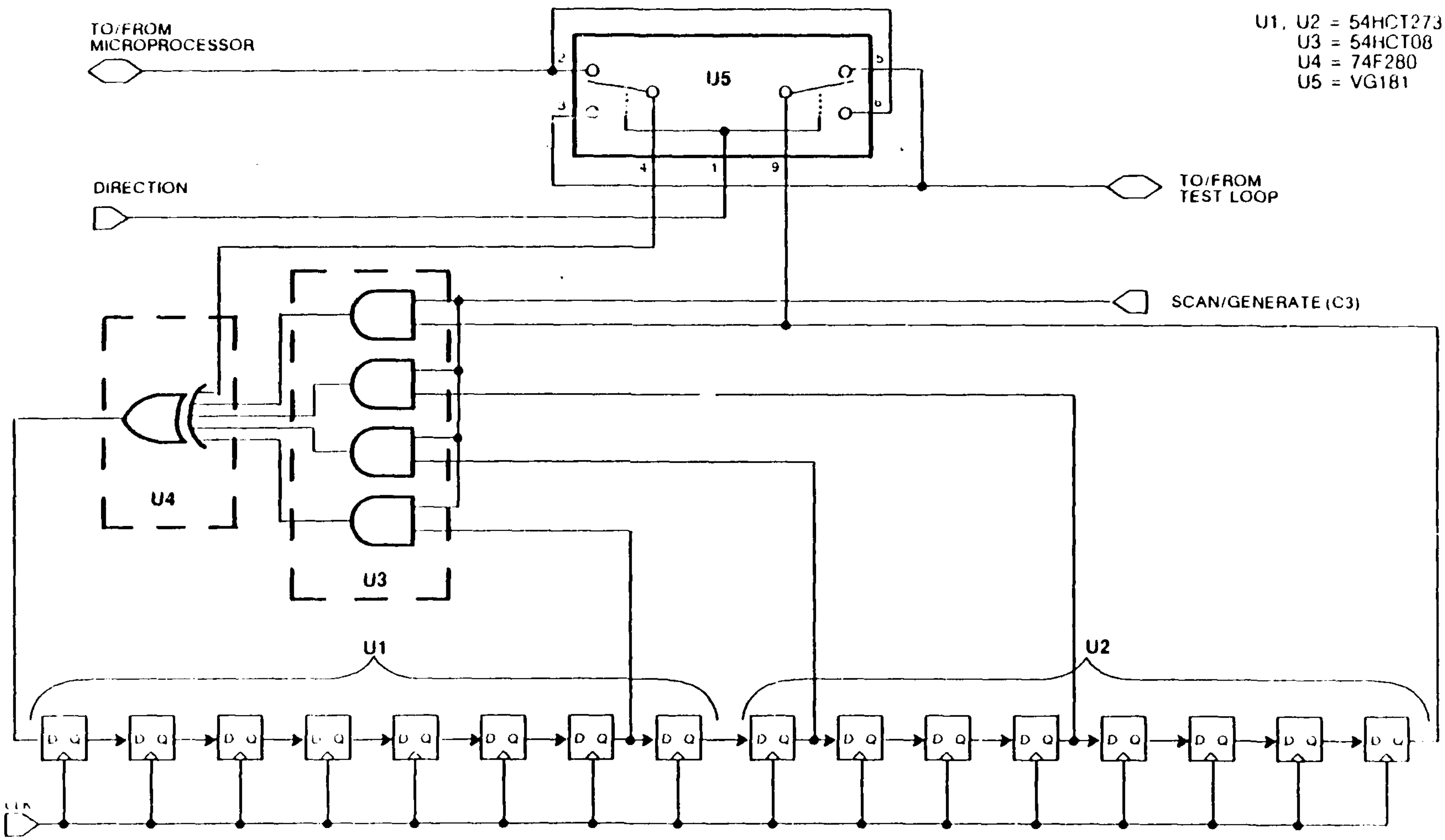


FIGURE 6 LEVEL III WIRING DIAGRAM
1 OF 4 SCAN/SET REGISTERS – DETAIL

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT

CATEGORY: LONG TUTOTIAL

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

NUMBER/NAME (Q)		AREA *(sq in)*	# OF PINS	POWER TYPICAL *(mW)*	POWER MAX. *(mW)*	WEIGHT *(gms)*
8051/8751	(1)	1.20	40	175.000	750.000	[illegible]
2817A	(1)	0.30	28	300.000	750.000	1.4
54HCT253	(1)	0.24	16	0.150	0.500	1.0
54HCT138	(1)	0.30	20	0.150	0.275	[illegible]
54LS373	(1)	0.30	20	0.135	0.200	[illegible]
SCAN / SET REGISTER COMPONENTS (FOUR REQUIRED)						
54HCT273	(2)	0.30	20	0.250	0.375	[illegible]
54F280	(1)	0.21	14	130.000	175.000	[illegible]
54HCT08	(2)	0.21	14	0.015	0.050	[illegible]
DG181	(1)	0.21	14	0.500	10.000	[illegible]
54HCT04	(1)	[illegible]	14	0.015	0.050	[illegible]
SCAN/SET TOTALS: (PER REGISTER)		1.65	110	130	185	6.7
GRAND TOTALS:		9.44	564	995	2,200	33.3

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIBLIOGRAPHY

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

1. V.R. Subramanyam, L. R. Stine, (TRW), "Design for Testability for Future Digital Avionics Systems", IEEE, 1986. Describes a Module Maintenance Node which is the basis for the Test Processor Node in the OBIVCB.

2. R. Frohwerk, "Signature Analysis: A New Digital Field Service Method", Hewlett-Packard, 1977. Includes a good tutorial on Linear Feedback Shift Registers.

3. LeBlanc, "LOCST - LSSD On Chip Self Test", IEEE Design & Test of Computers, 1984.

4. D. Bacht, "Understanding Signature Analysis", Electronics Test, Nov. '82, pg. 28.

5. B. Konemann, Joachim Mucha and Gunther Zwiehoff, "Built-in logic block observer", I.E.E.E. Test Conference, Cherry Hill, NJ, 1979.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT

CATEGORY: USER REQUESTED DATA | PAGE 1 of 1

SUBCATEGORY:

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

QUESTIONS	VARIABLE ASSIGNMENTS
1. What is the number of test loops beyond the four in minimal configuration needed?	v1
2. What is the number of parallel test lines in groups of eight, beyond the eight already provided?	v2
3. What is the pattern application rate?	v3
4. What is the number of test patterns stored in memory for parallel testing?	v4
5. What is the initialization time?	v5
6. What is the length of the Linear Feedback Shift Registers?	v6

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITION

n1 = Minimum configuration

v1 = Number of test loops needed beyond the four of the minimum configuration.

v2 = Number of parallel test lines in groups of 8 beyond the eight already provided.

v3 = Test Pattern application rate.

v4 = Number of Test Patterns stored in memory for parallel testing.

v5 = Initialization time.

v6 = Length of Linear Feedback Shift Registers.

II) COMPONENT DETERMINATION EQUATIONS

n1 = 1

III) PENALTY EQUATIONS

AREA (sq in)

Area of BIT chips = 9.44 n1 + 1.65 v1 + 0.30(v2)

Total area of BIT circuitry = Area of BIT chips + 15% For PC traces

= 1.15 (Area of BIT chips)

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ON-BOARD INTEGRATION OF VLSI CHIP BIT

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

III) PENALTY EQUATIONS (CONT)

WEIGHT (gms)

Weight of BIT chips = 33.3n1 + 6.7 v1 + (1) (v2)

POWER (mW)

POWER = (2.2)n1 + 0.185 v1 + 0.02 (v2) (Watts maximum)

TIME

TEST TIME = v5 + (v6)(v3) + (v3)(v4)

PARAGRAPH 6.5

BUILT-IN LOGIC BLOCK OBSERVER (BILBO) TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: SHORT TUTORIAL **PAGE** [illegible] **of** [illegible]

SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE

DATA TYPE: TEXT [X] LIST [ ] TABLE [ ] GRAPHIC [ ] EQUATIONS [ ]

DATA:

SHORT TUTORIAL
FOR
BILBO (MISR/PRPG) BIT

Built-In Logic Block Observer (BILBO) is a multifunctional circuit which can be configured as any of the following:

1. Latch
2. Linear shift register
3. Multiple Input Shift Register (MISR) or Pseudo Random Pattern Generation (PRPG)
4. Reset the register

Specific configurations are obtained by the application of 2 mode control bits. BILBO circuitry can be used to perform signature analysis using a pseudo random pattern generator (PRPG) and a multiple input signature register (MISR) which is an effective method of testing complex digital circuitry. The foundation of this Built-In-Test (BIT) technique is built on the fact that for a given set of stimuli, a Circuit Under Test (CUT) will output a particular digital stream. Using the data compression techniques of signature analysis, an output signature accumulated can be saved in a MISR. At the conclusion of the application of a given set of stimuli, the contents of the MISR are then compared against the known good signature. Initialization of the CUT and the BIT circuitry must be done prior to the execution of this technique. By utilizing the BILBO circuit, initialization can be easily achieved using scan-path techniques. The versatility of BILBO allows for the combination of a number BIT techniques, namely SCAN and MISR/PRPG. This combination is especially useful when testing combinational logic stages separated by latches. Some of these latches are replaced with a BILBO circuit. During normal operation, the BILBO is functionally identical to a latch.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: SHORT TUTORIAL | PAGE 2 of 5

SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE

DATA TYPE: TEXT [x] LIST [ ] TABLE [ ] GRAPHIC [ ] EQUATIONS [ ]

DATA:

SHORT TUTORIAL
FOR
BILBO (MISR/PRPG) BIT
(CONT)

During test initialization each BILBO is configured as a serial shift register, and an Exhaustive Test Initialization Pattern (ETIP) is shifted into the circuit. The BILBOs are then configured into a PRPG and MISR. This allows for complete testing of the CUT

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: SHORT TUTORIAL

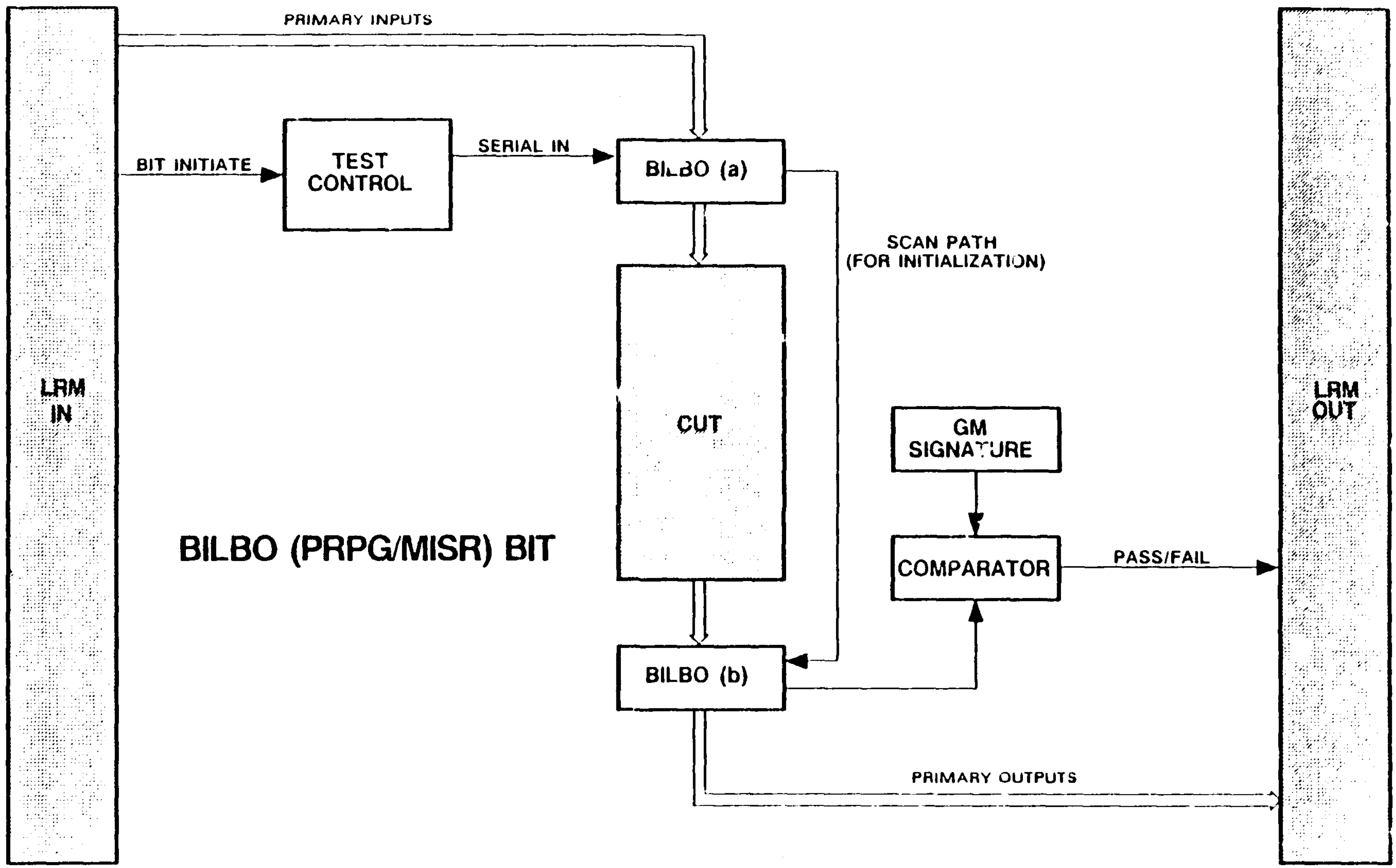
SUBCATEGORY:
1. LEVEL I BLOCK DIAGRAM
2. BIT SEQUENCE FLOW CHART

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2



UNSHADED BOXES REPRESENT BIT CIRCUITRY

FIGURE 1 LEVEL I BLOCK DIAGRAM BILBO (MISR/PRPG) BIT

PAGE 4 of 5

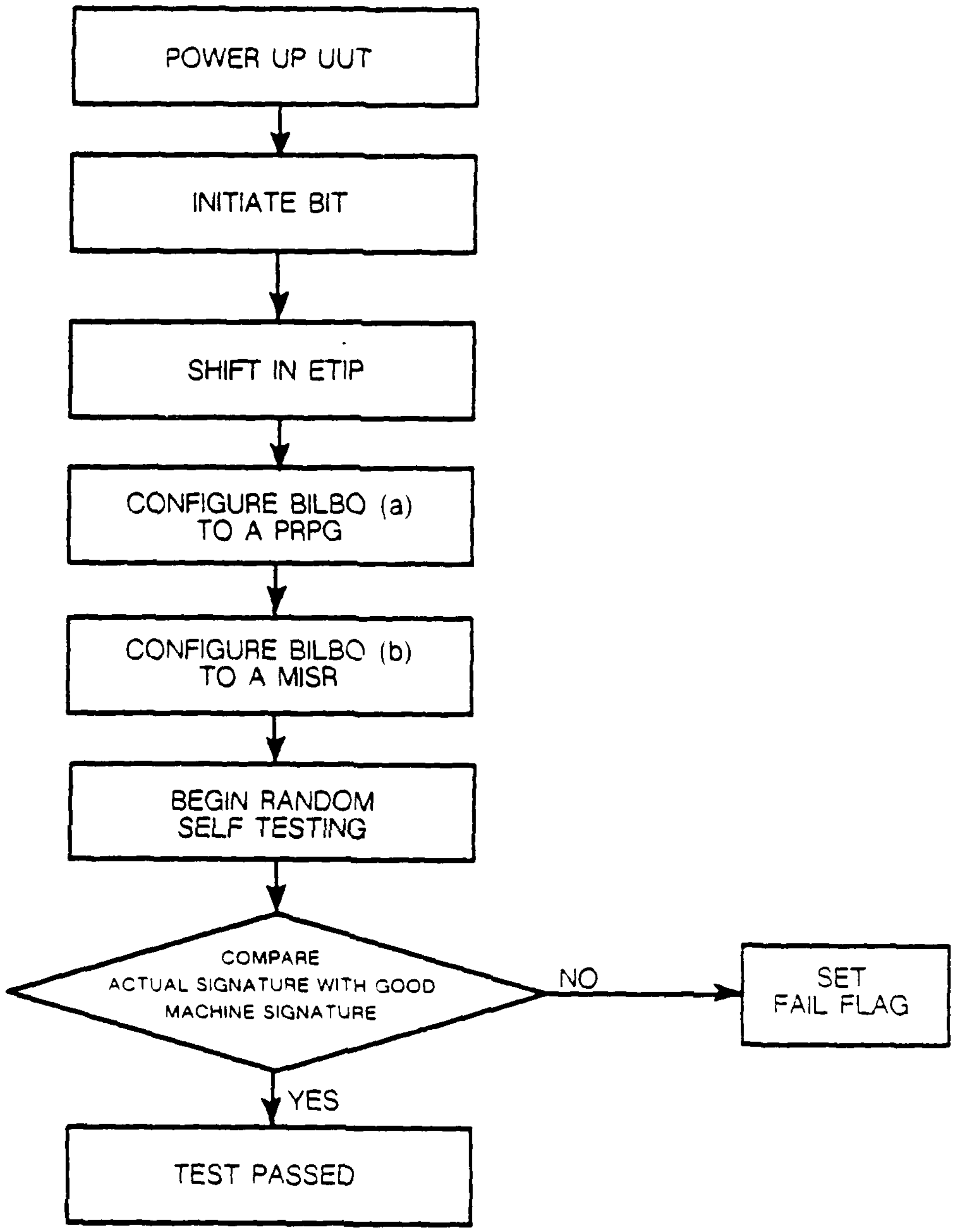


FIGURE 2 BIT SEQUENCE FLOW CHART
FOR BILBO (MISR/PRPG) BIT

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: LONG TUTORIAL | PAGE 1 of 11

SUBCATEGORY: BIT SEQUENCE FLOWCHART DESCRIPTION

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
BILBO (MISR/PRPG) BIT

1. Unit Under Test (CUT) is powered up.

2. An initiate BIT signal is generated.

3. Using the BILBOs as shift registers, an Exhaustive Test Initialization Pattern (ETIP) is scanned into the CUT.

4. BILBO(a) is configured to a Pseudo Random Pattern Generator (PRPG) and BILBO(b) is configured to a Multiple Input Signature Register (MISR).

5. Random testing is executed.

6. BILBO(b) now contains the CUT signature which is fed into the 8 bit comparator

7. If the CUT signature does not match the Good Machine (GM) signature, a failure flag is set. If the CUT signature matches the GM signature, the test passed

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BILBO (MISR/PRPG) BIT
ADVANTAGES

The BILBO (PRPG/MISR) BIT technique provides the following advantages to the circuit designer:

1. One circuit design can be used for multiple functions giving the advantages of commonality (custom integrated circuit design can be made and used in many places).
2. The versatility of BILBO allows the designer to combine the advantages of SCAN techniques with PRPG/MISR techniques.
3. The test data is gathered at the rated internal speed of the integrated circuits.
4. A much higher failure detection rate is achieved when compared to other techniques such as transition counting.
5. Minimal software support is required.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE DISADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BILBO (MISR/PRPG) BIT
DISADVANTAGES

The BILBO (PRPG/MISR) BIT technique poses the following disadvantages to the circuit designer:

1. BILBO must be incorporated in the CUT as part of the original design of the circuit.
2. BILBO modules are more complex than the latches they replace. This results in additional circuitry.
3. Limited Test Vector Set which is more effective with high amount of combinational logic circuitry.
4. Circuit throughput delay will increase if BILBO is used as an input or output register.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT	
CATEGORY: LONG TUTORIAL	**PAGE** 4 **of** 11
SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BILBO (MISR/PRPG) BIT
ATTRIBUTES

1. REAL ESTATE PENALTY
   - BILBO modules latches are more complex and take up more area than the conventional latches they replace.
   - Some test control logic is also required.
   - The comparator which compares the good machine signature to the actual signature takes up area.
2. POWER PENALTY
   - Proportional to the power dissipated by the test control logic, the additional circuitry of the BILBO module and the comparator.
3. RELIABILITY PENALTY
   - Proportional to the Mean Time Between Failures (MTBF) of the Test Control Logic, the BILBO module and the comparator.
4. TIMING PENALTY
   - Operation speed is slowed due to the following:
     - Propagation delay through the data inputs AND gates on the BILBO cell.
5. CONCEPTUAL COMPLEXITY
   - Circuit design is moderate in complexity.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: LONG TUTORIAL | **PAGE** 5 **of** 11

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BILBO (MISR/PRPG) BIT
ATTRIBUTE
(CONT)

6. TECHNOLOGY

   • All current digital technologies

7. IS BITE SELF TESTABLE?

   • Yes, with additional hardware.

8. DESIGN COST

   • All components used are readily available at low cost.

   • Hardware design and debug is minimal.

10. WEIGHT

   • Proportional to the weight of the test control logic, the additional circuitry of the BILBO module and the comparator.

LIBRARY ELEMENT DATA SHEET

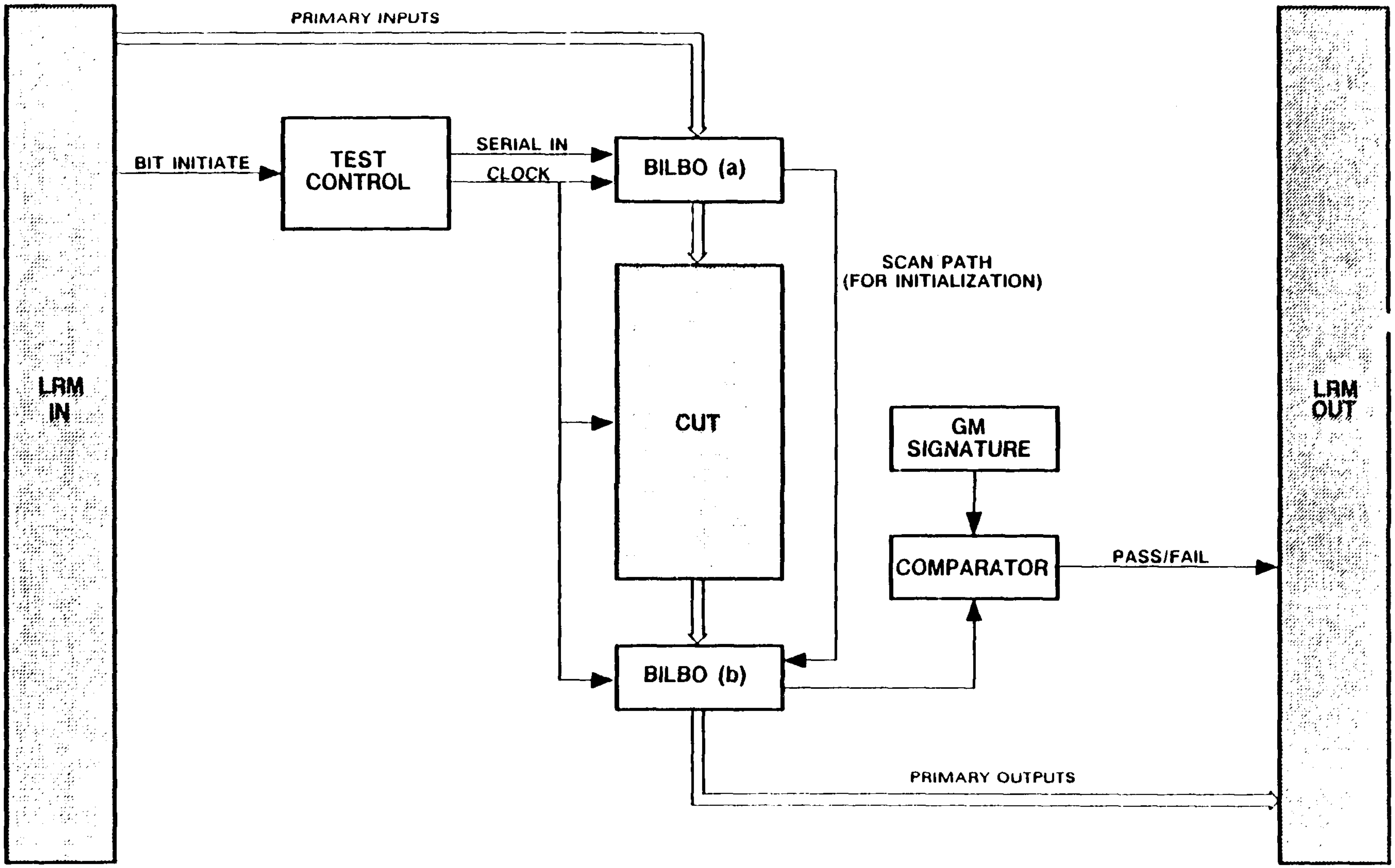
BIT TECHNIQUE: BILBO (MISR/PRPG) BIT	
CATEGORY: LONG TUTORIAL	**PAGE** 6 **of** 11
SUBCATEGORY: DEFAULT DESIGN	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

a) SEE FIGURE 3 BILBO (MISR/PRPG) BIT LEVEL II BLOCK DIAGRAM

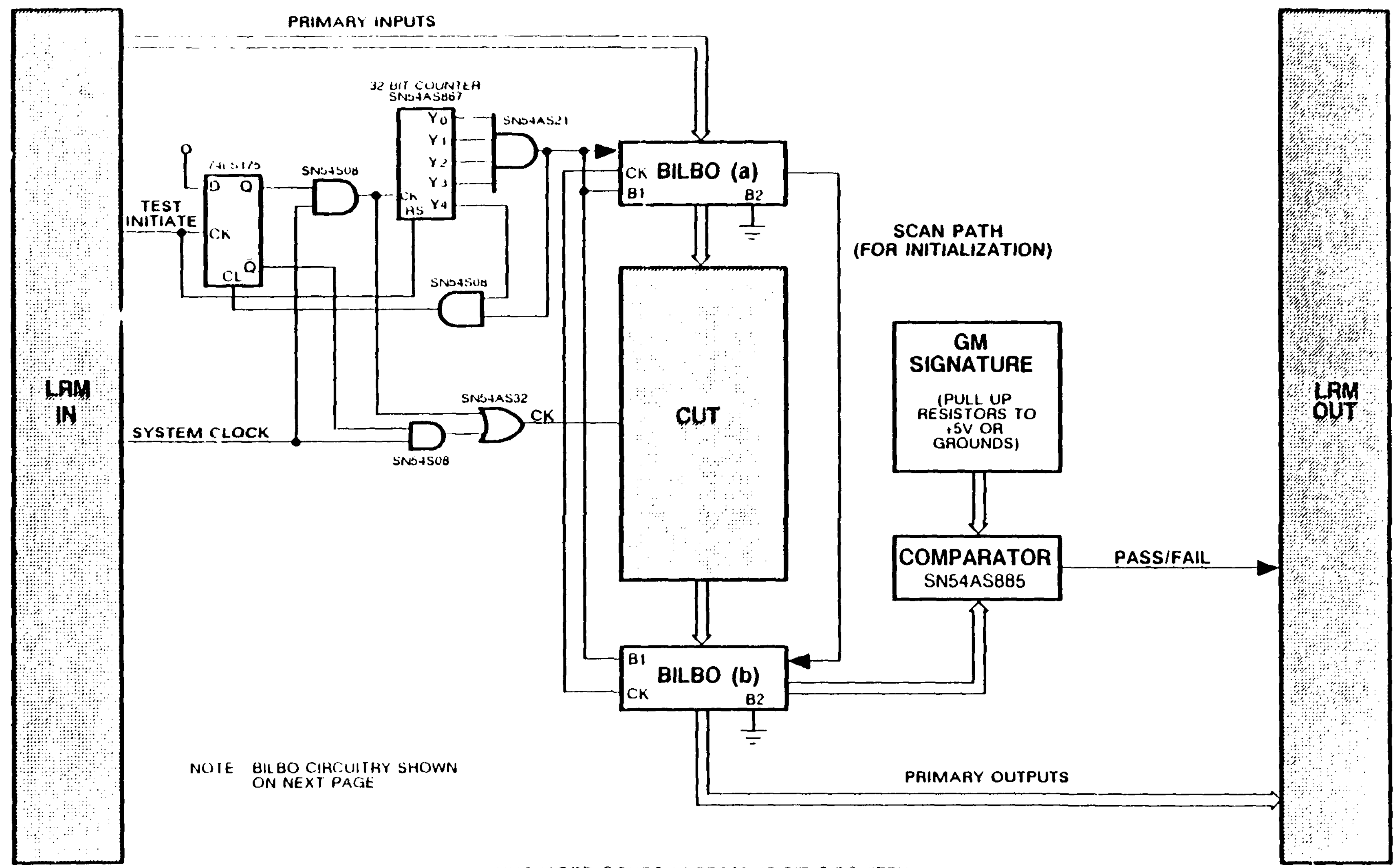
b) SEE FIGURE 4 BILBO (MISR/PRPG) BIT DEFAULT DESIGN

c) SEE FIGURE 5 BILBO (MISR/PRPG) BIT MODULE



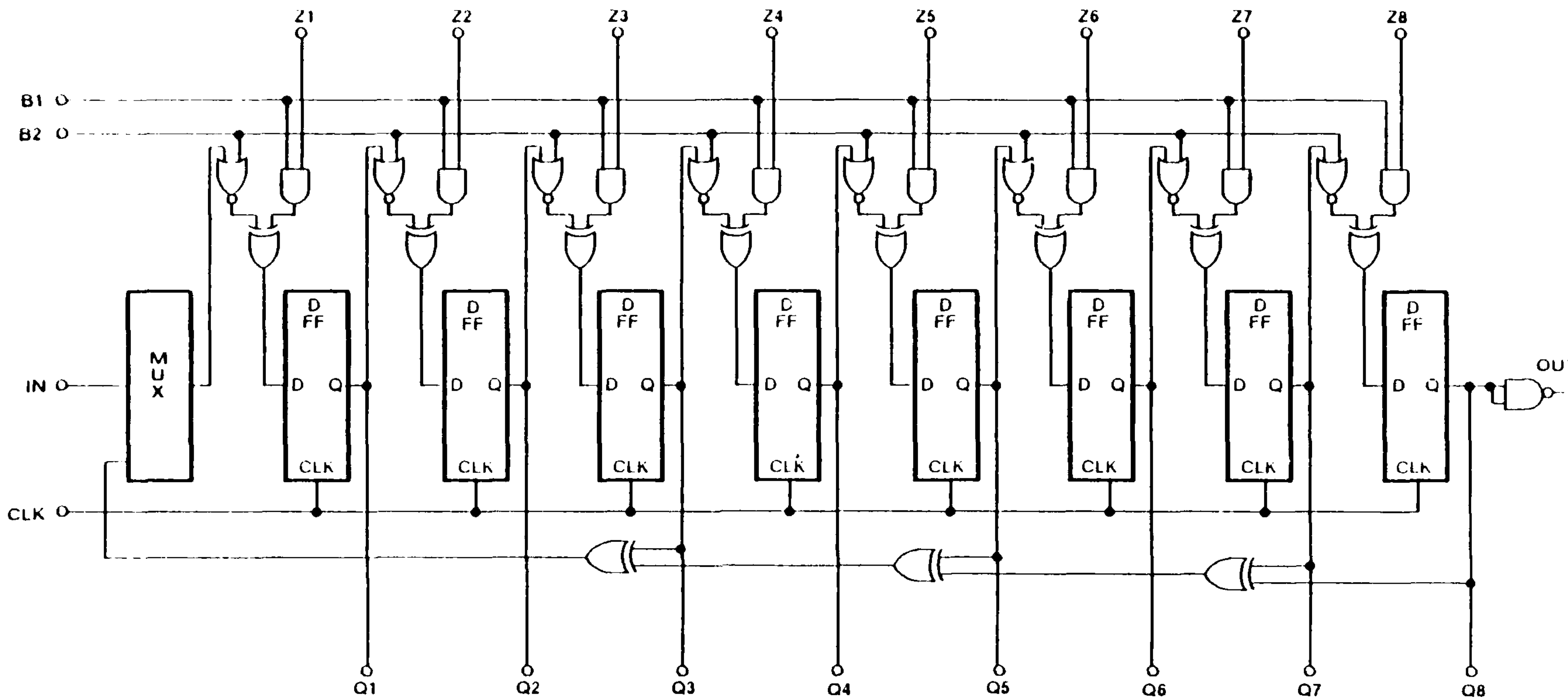
UNSHADED BOXES REPRESENT BIT CIRCUITRY

FIGURE 3 LEVEL II BLOCK DIAGRAM
BILBO (MISR/PRPG) BIT



UNSHADED BOXES REPRESENT BIT CIRCUITRY

FIGURE 4 DEFAULT DESIGN
BILBO (MISR/PRPG) BIT



THE SETTING OF THE INPUTS B1 AND B2 DETERMINES HOW THE BILBO IS CONFIGURED. (SEE TABLE BELOW).

B1	B2	BILBO CONFIGURATION
0	0	LINEAR SHIFT REGISTER
0	1	RESET THE BILBO
1	0	PRPG/MISR
1	1	LATCH

FIGURE 5 BILBO (MISR/PRPG) BIT MODULE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: LONG TUTORIAL | **PAGE** 10 of 11

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

NUMBER/NAME	AREA (sq in)	# OF PINS	POWER TYPICAL (mW)	POWER MAX. (mW)	WEIGHT (gms)
74LS175/ D FLIP FLOP	0.20	16	60	90	[illegible]
SN54AS08/ AND CHIP	0.24	14	260	440	[illegible]
SN54AS21/ AND CHIP	0.23	14	300	540	[illegible]
SN54AS32/ OR CHIP	0.23	14	300	540	[illegible]
SN54AS885/ COMPARATOR	0.37	24	50	85	[illegible]
SN54AS867/ 8 BIT COUNTER	0.37	24	44	125	[illegible]
54LS33/ NOR	0.23	14	300	540	[illegible]
54LS86/ EXOR	0.23	14	300	540	
SN54ALS01 NAND	0.23	14	300	540	[illegible]

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIBLIOGRAPHY

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BILBO - Built-In Logic Block Observation Techniques

79 - Koenemann, Mucha, Zwieoff - 1979 IEEE Test Conference

81 - Segers - 1981 IEEE Test conference -
A Self-Test Method for Digital Circuits

STUMPS - Self Testing of Multi Chip Logic Modules

82 - Bardell, McAnney - 1982 IEEE Test Conference

83 - Komonysky - Electronics 1983 -
Synthesis of techniques creates complete system self-test

84 - Butt, El-ziq - 1984 International Test Conference -
Impact of Mixed-Mode Self-Test On Life Cycle Cost Of VLSI Based Designs

85 - Bhavsar - 1985 International Test Conference -
"Concatenable Polydividers", Bit-Sliced LFFSR Chips For Board Self-Test

85 - Kraniewski, Albicki - "Self-Testing Pipelines"

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: USER REQUESTED DATA | **PAGE** 1 of 1

SUBCATEGORY:

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

QUESTIONS	VARIABLE ASSIGNMENTS
1. How many inputs?	v1
2. How many outputs?	v2
3. What is the operating speed of the system clock?	v3
4. What is the CUT initialization time?	v4
5. How many test patterns will be applied?	v5

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: EQUATIONS | **PAGE** 1 **of** 3

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITION

n1 = Number of FLIP FLOP chips

n2 = Number of 2 input AND chips

n3 = Number of 4 input AND chips

n4 = Number of 2 input OR chips

n5 = Number of 8 bit COMPARATOR chips

n6 = Number of COUNTERS

n7 = Number of BILBO AND gates

n8 = Number of BILBO NOR gates

n9 = Number of BILBO NAND gates

n10 = Number of BILBO EXOR gates

n11 = Number of BILBO FEEDBACK EXOR gates

n12 = Number of NOR chips

n13 = Number of EXOR chips

n14 = Number of NAND chips

v1 = Number of CUT inputs

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT	
CATEGORY: EQUATIONS	**PAGE** 2 **of** 3
SUBCATEGORY: (DATA NOT TO BE DISPLAYED)	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒	

DATA:

I) VARIABLE DEFINITION (CONT)

v2 = Number of CUT outputs

v3 = System clock speed

v4 = CUT initialization time

v5 = Number of test patterns

II) COMPONENT DETERMINATION EQUATIONS

n1 = 1

n2 = Integer [(3 + v1 +v2)/4 + 0.99]

n3 = 1

n4 = 1

n5 = Integer [v2/8 + 0.99]

n6 = 1

n7 = v1 + v2

n8 = v1 + v2

n9 = 2

n10 = v1 + v2

n11 = Integer [Natural Log (v1 + v2)/Natural Log 2 + 0.99]

n12 = Integer [(v1 + v2)/4 + 0.99]

n13 = Integer [(n10 + n11)/4 + 0.99]

n14 = 1

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: BILBO (MISR/PRPG) BIT

CATEGORY: EQUATIONS | **PAGE** 3 **of** 3

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: **TEXT** ☐ **LIST** ☐ **TABLE** ☐ **GRAPHIC** ☐ **EQUATIONS** ☒

DATA:

III) PENALTY EQUATIONS

a) AREA (sq in)

AREA OF BIT CHIPS $= .2n1 + .24n2 + .23n3 + .23n4 + .37n5 + .37n6 + .23n12 + .23n13 + .23n14 = 1.26 + .24n2 + .37n5 + .23(n12 + n13)$

TOTAL AREA OF BIT CIRCUITRY = (Area of BIT chips) + 15% for PC traces $= 1.45 + 1.15\,[.24n2 + .37n5 + .23(n12 + n13)]$

b) WEIGHT (gms)

WEIGHT OF BIT CHIPS $= .9n1 + 1.1n2 + 1.1n3 + 1.1n4 + 1.6n5 + 1.6n6 + 1.1n12 + 1.1n13 + 1.1n14 = 5.8 + 1.1(n2 + n12 + n13) + 1.6n5$

TOTAL WEIGHT OF BIT CIRCUITRY = (Weight of BIT chips) + (10% FOR Weight of solder) $= 5.8 + 1.1(n2 + n12 + n13) + 1.6n5 + .1(5.8 + 1.1)(n2 + n12 + n13) + 1.6n5) = 6.4 + 1.1\,[1.1(n2 + n12 + n13) + 1.6n5)]$

c) POWER (mW)

TOTAL POWER CONSUMPTION OF BIT CHIPS $= 60n1 + 260n2 + 300n3 + 300n4 + 50n5 + 44n6 + 300n12 + 300n13 + 300n14 = 1004 + 260n2 + 50n5 + 300(n12 + n13)$

d) TEST TIME

TEST TIME $= v4 + (v5)(v3)$

PARAGRAPH 6.6

ERROR DETECTION AND CORRECTION CODES TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES	
CATEGORY: SHORT TUTORIAL	**PAGE** 1 of 4
SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE	
DATA TYPE: TEXT ☒ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

SHORT TUTORIAL
FOR
ERROR DETECTION AND CORRECTION CODES

Used as a concurrent Built-In-Test (BIT) Technique, Error Detection and Correction units provide greater memory system reliability through their ability to detect and correct memory errors. Using similar techniques as parity, Hamming codes generate extra encoding bits and appends them to the data word which is to be transmitted or stored in memory. When the data and extra encoding bits are read from memory, a new set of code bits are generated. Write check bits are generated when data is written into the memory, while read check bits are generated when data is read from memory. Each is derived from parity generators. Comparison is done by exclusive-or operation, and like parity, the result of the comparison, called the syndrome word, contains information to determine if an error occurred. Unlike parity, the syndrome word also contains information to indicate which bit is in error. After decoding this information, a flag can be set to indicate if an error occurred. Error correction with single bit errors is accomplished by inverting the bit in error. Identification of the bit in error by the syndrome word is provided by the binary value of the bit position.

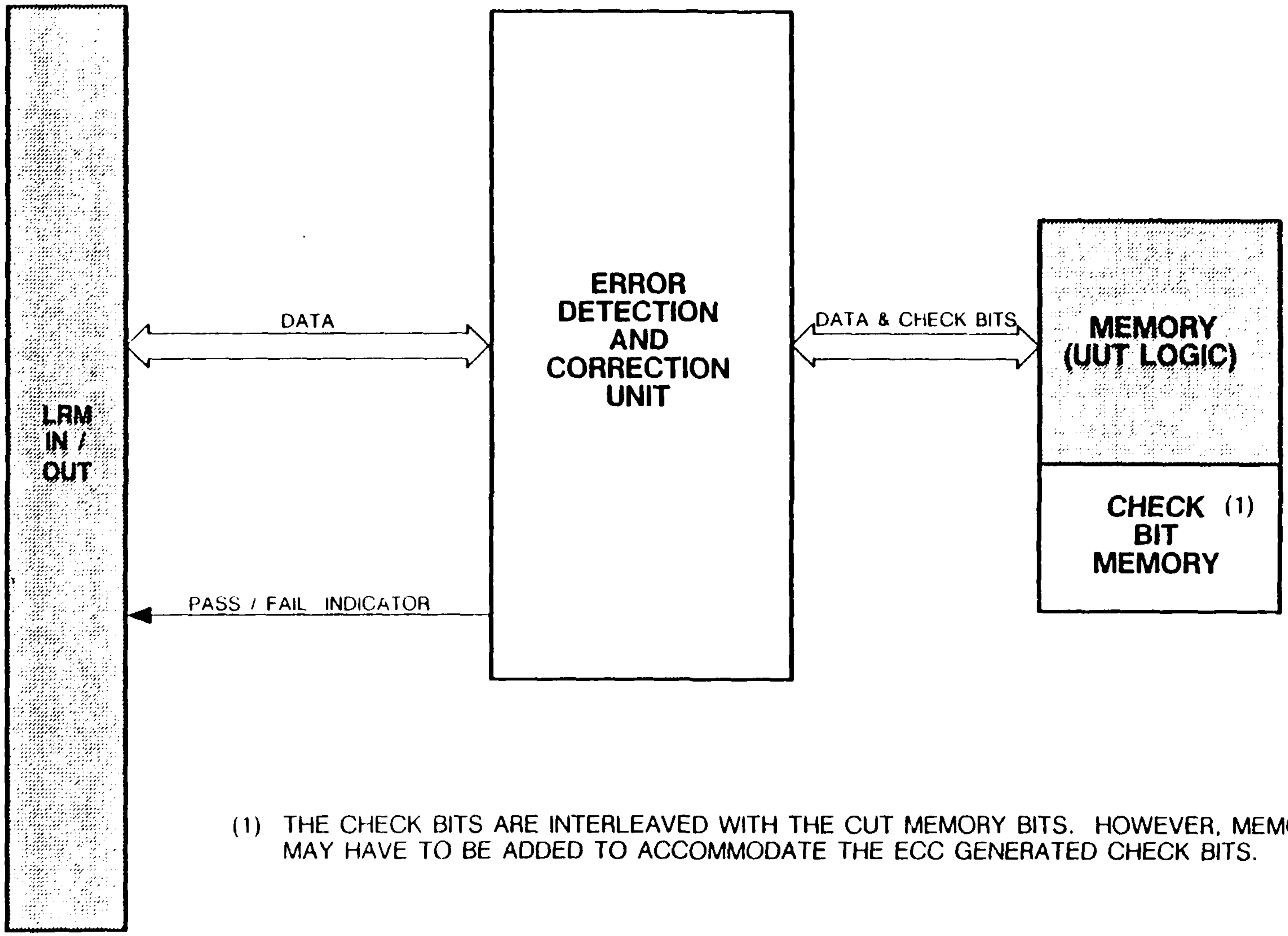
LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES	
CATEGORY: SHORT TUTORIAL	**PAGE** 2 of 4
SUBCATEGORY: 1. LEVEL I BLOCK DIAGRAM 2. BIT SEQUENCE FLOW CHART	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2



(1) THE CHECK BITS ARE INTERLEAVED WITH THE CUT MEMORY BITS. HOWEVER, MEMORY CHIPS MAY HAVE TO BE ADDED TO ACCOMMODATE THE ECC GENERATED CHECK BITS.

FIG 1 LEVEL I BLOCK DIAGRAM
ERROR DETECTION AND CORRECTION CODES

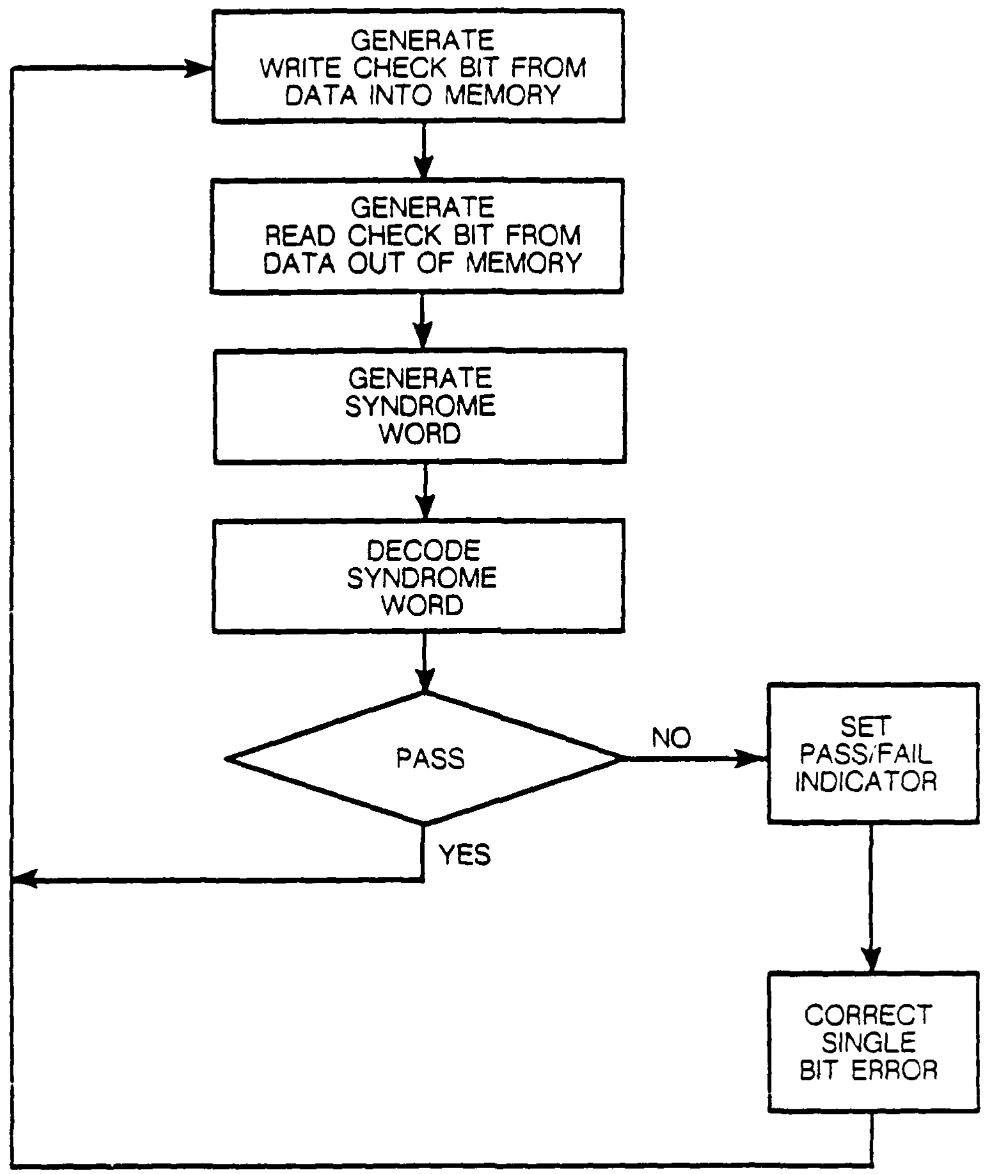


FIGURE 2 BIT SEQUENCE FLOW CHART FOR ERROR DETECTION AND CORRECTION CODES

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES		
CATEGORY: LONG TUTORIAL		PAGE 1 of 10
SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION		

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
ERROR DETECTION AND CORRECTION CODES

1. Generate write check BIT from data into memory of Unit Under Test (UUT) logic.

2. Generate read check BIT from data out of memory.

3. Generate syndrome word by exclusive-or operation of the fetched check BIT and the regenerated check BIT.

4. Decode the syndrome word to determine which BITs are in error.

5. Set FAIL indicator if error flag is set.

6. Correct the detected BIT error and send to Line Replaceable Module (LRM) output.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES	
CATEGORY: LONG TUTORIAL	**PAGE** 2 **of** 10
SUBCATEGORY: BIT SEQUENCE ADVANTAGES	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ERROR DETECTION AND CORRECTION CODES
ADVANTAGES

1. Error detection and correction code can ensure that memory systems reliability be increased. Read or write errors produced in memory can be corrected using this technique, therefore creating an overall better system reliability.

2. Relatively small amount of hardware required to use error detection as an error detection and correction code.

3. All in one chips available to accomplish error detection and correction.

4. Error Correction Code (ECC) chips can be cascaded for expanded word length.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES

CATEGORY: LONG TUTORIAL | **PAGE** 3 **of** 10

SUBCATEGORY: BIT SEQUENCE DISADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ERROR DETECTION AND CORRECTION CODES
DISADVANTAGES

1. Efficiencies of single detect and single detect / single correct codes decreases as the number of data bits increases.

2. Possible large hardware requirement for interfacing with large memory circuits.

3. Some decrease in throughput due to extra processing.

4. Requires addition of Random Access Memory (RAM) for check bits unless original cut memory design has sufficient number of spare bits. Some memory configurations could double the number of RAM chips required.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
ATTRIBUTES

1. REAL ESTATE PENALTY
   - Dependent on number of ECC chips. Number of ECC chips are proportional to word length. Therefore minimal impact if small word and large memory depth.
   - Dependent on number of added memory chips. This is a function of both width and depth. Could double the required area.
2. POWER PENALTY
   - (Number of ECC chips) x (ECC chip power) + (Number of memory chips) x (memory chip power).
   - Can be reduced if low standby power memory chips are used.
3. RELIABILITY PENALTY
   - Slight decrease of reliability due to addition of a small number of ECC chips. Becomes negligible for memories with very large number of words.
4. TIMING PENALTY
   - Slight increase in processing time - 80 nsec typical TTL
5. CONCURRENT
6. CONCEPTUAL COMPLEXITY
   - Straight forward.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
ATTRIBUTES
(CONT)

7. HARDWARE/SOFTWARE/COMBO

   - Hardware

8. TECHNOLOGY

   - If ECC integrated circuits are not available in a particular technology, ECC can be implemented in random integrated circuits with increasing penalty in real estate, and power.

9. IS BITE SELF TESTABLE?

   - Can be with additional hardware but would be costly in terms of penalty.

10. DESIGN COST

    - Minimal if ECC integrated circuits are used.

11. STAND-ALONE (SELF CONTAINED BIT?)

    - YES, If fault is in ECC integrated circuit, error flag will be detected unless fault is in error flag output.

12. WEIGHT

    - Weight penalty = (number of ECC integrated circuits) multiplied by (ECC integrated circuits) multiplied by (ECC weight) plus (number of memory integrated circuits) multiplied by (memory integrated circuit weight)

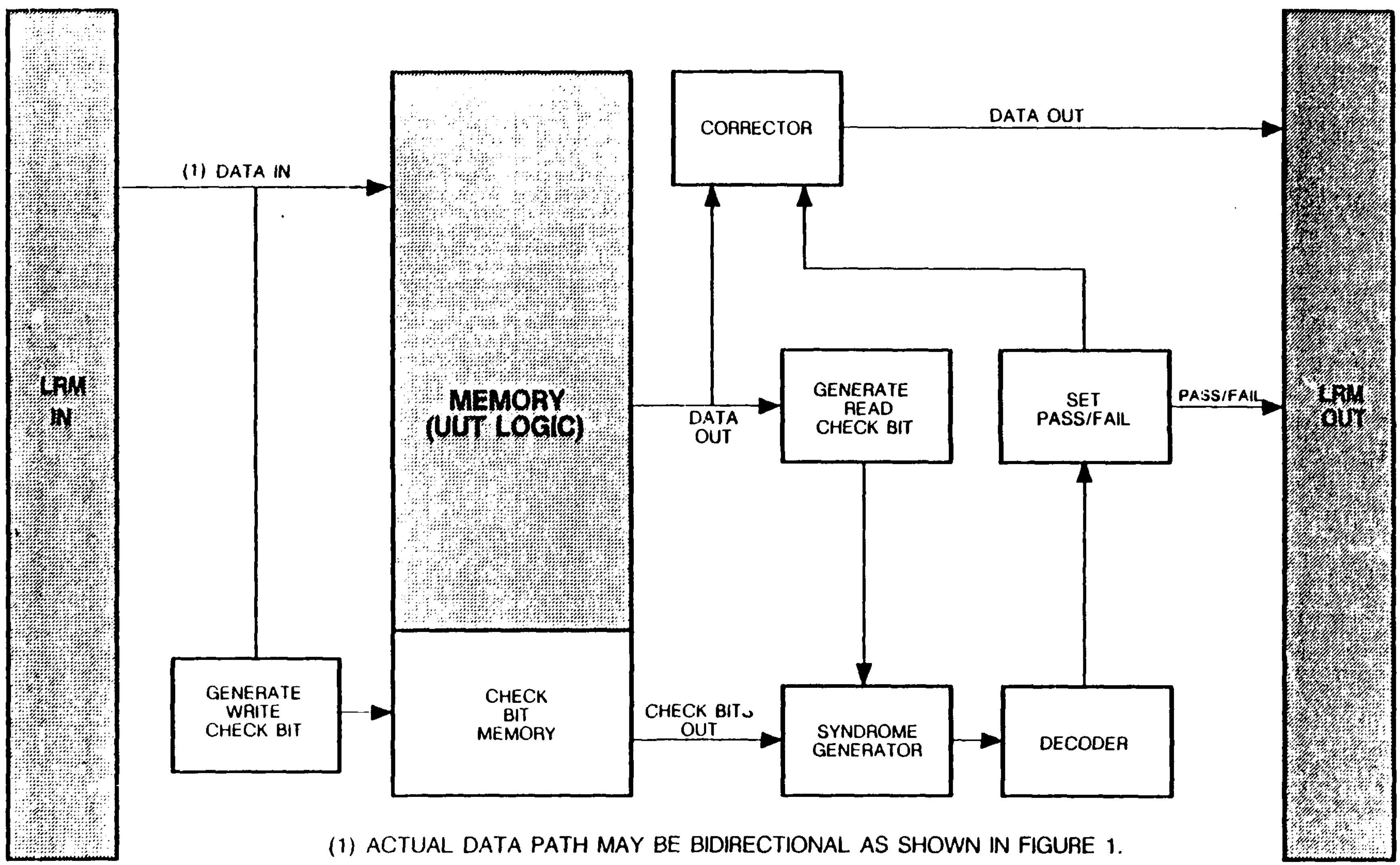
LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES	
CATEGORY: LONG TUTORIAL	**PAGE** 6 **of** 10
SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

a) SEE FIGURE 3 FOR ERROR DETECTION AND CORRECTION CODES BIT LEVEL II BLOCK DIAGRAM

b) SEE FIGURE 4 FOR ERROR DETECTION AND CORRECTION CODES BIT DEFAULT DESIGN



(1) ACTUAL DATA PATH MAY BE BIDIRECTIONAL AS SHOWN IN FIGURE 1.

FIGURE 3 LEVEL II BLOCK DIAGRAM
ERROR DETECTION AND CORRECTION CODES

PAGE 7 of 10

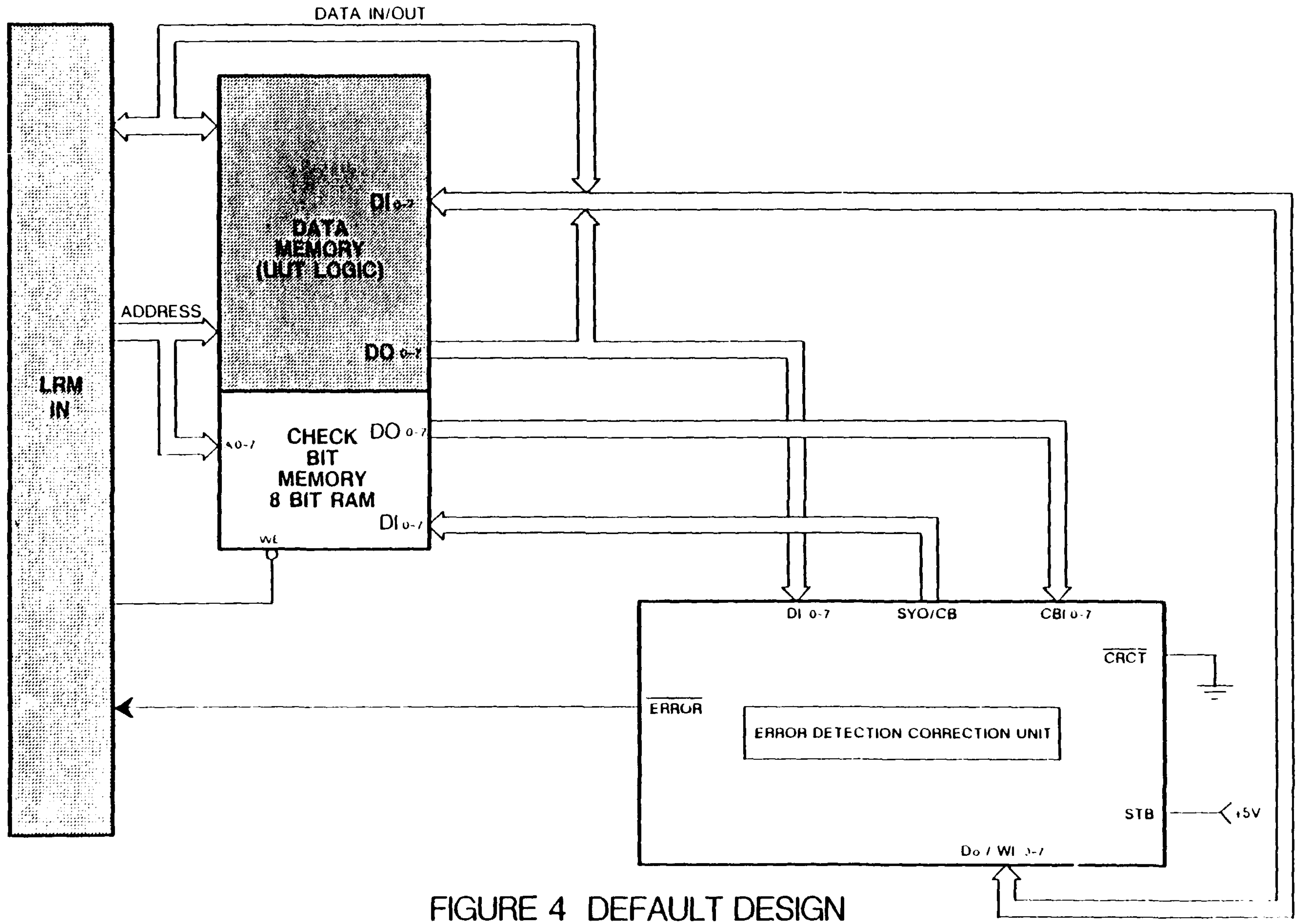


FIGURE 4 DEFAULT DESIGN
ERROR DETECTION & CORRECTION CODES BIT

PAGE 8 of 10

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES

CATEGORY: LONG TUTORIAL

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

NUMBER/NAME	AREA *(sq in)*	# OF PINS	POWER TYPICAL	POWER MAX. *(mW)*	WEIGHT *(gms)*
8206 (ECC)	1.20	68	175	750	1.7
81C28 (RAM)	0.80	24	50	150	1.1

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES	
CATEGORY: LONG TUTORIAL	**PAGE** 10 **of** 10
SUBCATEGORY: BIBLIOGRAPHY	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

1. Len Levine and Ware Meyers, "Semiconducting Memory Reliability with Error Detecting and Correcting codes," COMPUTER, October 1976, pp 43-50.2.

2. Intel application notes AP-73, "Memory System Reliability With ECC". Intel Memory Components Handbook 1985.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES

CATEGORY: USER REQUESTED DATA — **PAGE** 1 of 1

SUBCATEGORY:

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

QUESTIONS	VARIABLE ASSIGNMENTS
1. How many data bits are being read from memory?	v1
2. How many memory locations are required?	v2
3. What is the delay in throughput caused by the ECC circuit?	v3
4. What is the number of check bits required?	v4

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITION

$n1$ = Number of ECC chips where each unit can handle maximum 16 data bits with a maximum of 5 cascaded units for 80 data bits.

$n2$ = Number of memory chips

$v1$ = Number of data bits

$v2$ = Number of cut memory locations

$v3$ = Throughput delay of ECC circuit

$v4$ = Number of check bits required

II) COMPONENT DETERMINATION EQUATIONS

$n1 = v1/16$

$n2 = (v4/8)(v2/2K)$

III) PENALTY EQUATIONS

a) AREA (sq in)

Area of BIT chips = $(.640)n1 + (0.21)n2$

Total area of BIT Circuitry = (Total area of BIT chips)
+ 15% For PC traces.
= 1.15 (Area of BIT chips)

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ERROR DETECTION AND CORRECTION CODES

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

III) PENALTY EQUATIONS (CONT)

c) POWER (Watts)

POWER = (1.5)n1 + (150)n2

d) TIME

THROUGHPUT DELAY = v3

b) WEIGHT (gms)

Weight of BIT circuitry = Weight of BIT chips + Weight of memory chips
+ 10% For weight of solder.
= 1.1 (Weight of chips)

PARAGRAPH 6.7

SCAN TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES	
CATEGORY: SHORT TUTORIAL	**PAGE** 1 **of** 4
SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE	

DATA TYPE: **TEXT** [X] **LIST** [ ] **TABLE** [ ] **GRAPHIC** [ ] **EQUATIONS** [ ]

DATA:

SHORT TUTORIAL
FOR
SCAN DESIGN TECHNIQUES

SCAN design technique provides easy access of buried sequential circuit elements. SCAN design adds hardware overhead yet has gained widespread popularity due to the following testability attributes it provides.

OBSERVABILITY: The ability to read the state of an entire Line Replaceable module (LRM) to a specified applied test pattern.

CONTROLABILITY: The ability to initialize a Circuit Under Test (CUT) containing sequential memory elements with more complex test patterns than presets and clears can provide.

PARTITIONING: A SCAN chain becomes a natural partition between logic clusters thereby promoting the divide and test approach to testing.

By utilizing such circuits as a serial shift register, the SCAN technique is easily accomplished. In bit-serial SCAN/SET, the nodes to be scanned are parallel-shifted into a bit-serial register and then serially shifted out for inspection by the maintenance processor. If the inspection data does not match a good machine state, a PASS FAIL indicator can be set. The subject technique describes a SCAN/SET implementation. Other types of SCAN are:

- Level Sensitive Scan Design (LSSD)
- Random Addressable Scan
- Boundary Scan

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES	
CATEGORY: SHORT TUTORIAL	**PAGE** 2 of 4
SUBCATEGORY: 1. LEVEL I BLOCK DIAGRAM 2. BIT SEQUENCE FLOW CHART	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2

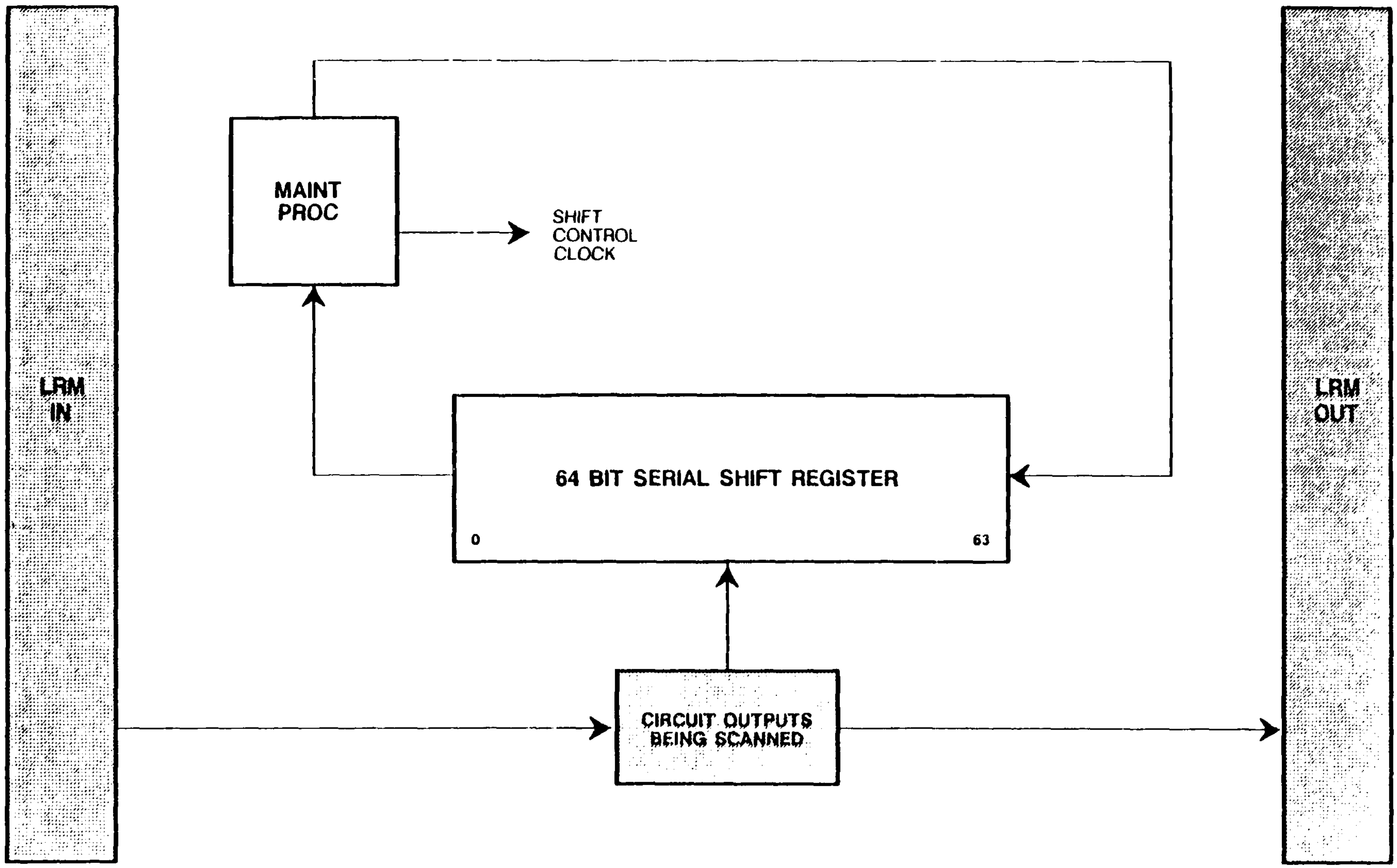


FIGURE 1 LEVEL I BLOCK DIAGRAM
SCAN BIT TECHNIQUE

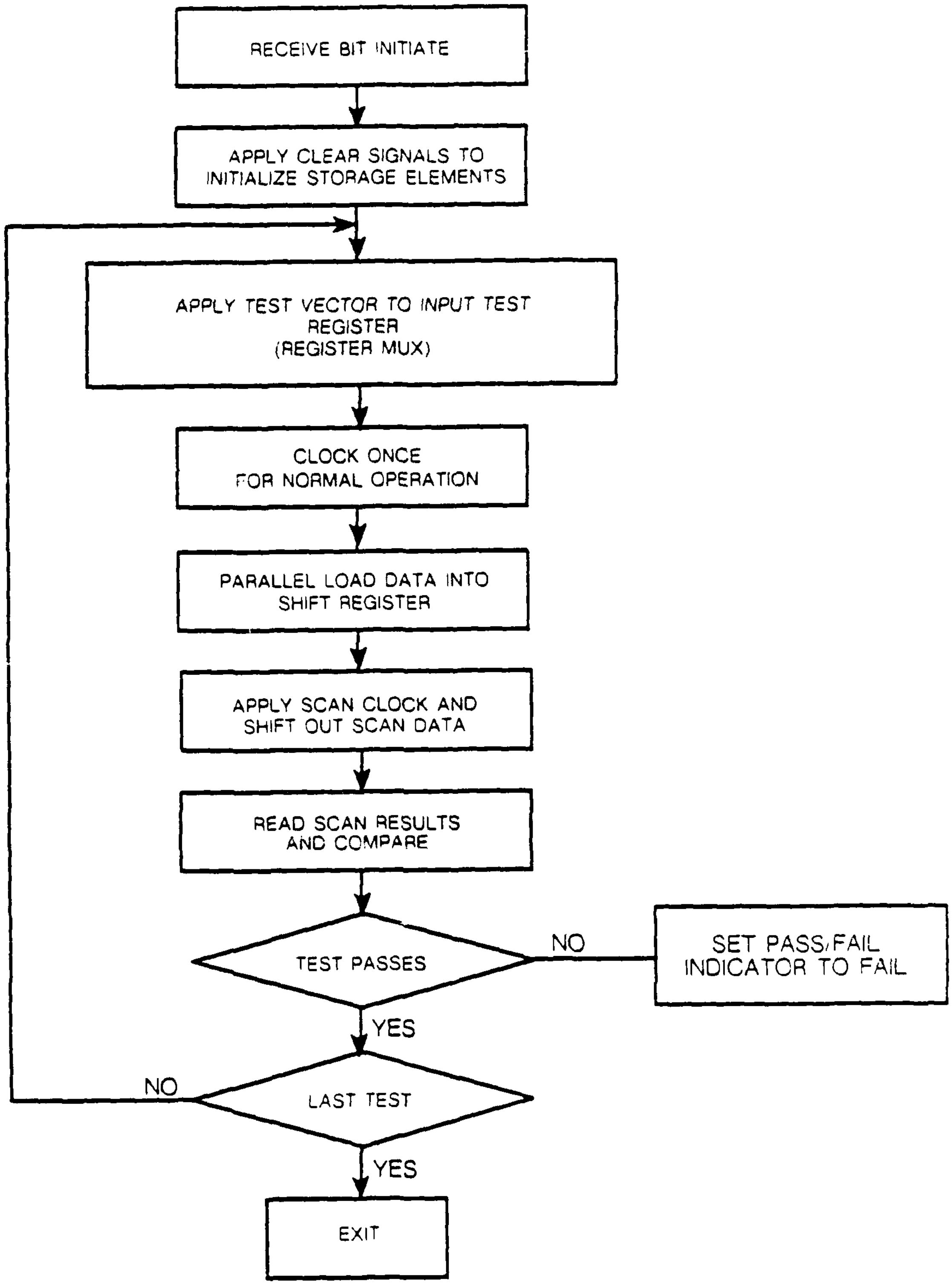


FIGURE 2 BIT SEQUENCE FLOW CHART
FOR SCAN BIT TECHNIQUE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES	
CATEGORY: LONG TUTORIAL	**PAGE** 1 **of** 12
SUBCATEGORY: BIT SEQUENCE FLOWCHART DESCRIPTION	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
SCAN DESIGN TECHNIQUES

1. Receive bit initiate and set test inputs.
2. Apply test vectors to input test register (register/multiplexer).
3. Clock once for normal operation.
4. Parallel load data into shift registers.
5. Apply SCAN clock and shift out SCAN data.
6. Read SCAN results and compare.
7. If test fails set PASS/FAIL indicator.
   If test passes continue on to next test or finish.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ADVANTAGES

DATA TYPE: TEXT [ ] LIST [X] TABLE [ ] GRAPHIC [ ] EQUATIONS [ ]

DATA:

SCAN DESIGN TECHNIQUES
ADVANTAGES

1. SCAN/SET latches completely external to CUT.
2. Allows for parallel load/serial SCAN out and serial in/parallel sets modes of operation.
3. Only one maintenance clock is required.
4. Possible to take system "SNAPSHOTS".

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE DISADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

SCAN DESIGN TECHNIQUES
DISADVANTAGES

1. Serial in and serial out modes still require large amount of test time.

2. Requires control of system clock.

3. Requires maintenance processor for control.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES	
CATEGORY: LONG TUTORIAL	PAGE 4 of 12
SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

SCAN DESIGN TECHNIQUES
ATTRIBUTES

1. REAL ESTATE PENALTY
   - Dependent on number of SCAN registers. (One register stage for each CUT flip flop.) Also dependent on number of CUT inputs.
2. POWER PENALTY
   - Power penalty will depend on the number of SCAN registers and the processor chip power.
3. RELIABILITY
   - Slight decrease of reliability due to addition of a small number of register chips. Becomes negligible for very large combinational CUT circuitry.
4. TIMING PENALTY
   - Slight increase in processing time - 80 nsec typical Transistor Transistor Logic (TTL).
   - Long BIT test time because of serial data transfer.
5. NOT CONCURRENT
6. CONCEPTUAL COMPLEXITY
   - Moderately complex.
7. HARDWARE/SOFTWARE/COMBO
   - Hardware.
   - Software in maintenance processor.
8. TECHNOLOGY
   - All current technolgies.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

SCAN DESIGN TECHNIQUES
ATTRIBUTES
(CONT)

9. IS BIT SELF TESTABLE?
   - Maintenance processor can run self test. Shift registers can be serially loaded then read out.
10. DESIGN COST
    - Minimal with off the shelf chips available. Additional cost for maintaining processor. However, one of the maintenance processors is designed so it can be used on other LRMs.
11. STAND-ALONE (self contained BIT?)
    - Yes
12. WEIGHT PENALTY
    - Roughly proportional to real estate penalty. Higher if CUT has large number of flip flop to be monitored and large number of inputs.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES

CATEGORY: LONG TUTORIAL

SUBCATEGORY: DEFAULT DESIGN

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐

DATA:

a) SEE FIGURE 3 LEVEL II BLOCK DIAGRAM SCAN BIT TECHNIQUE (SET)

b) SEE FIGURE 4 DEFAULT DESIGN (SCAN/SET)

c) SEE FIGURE 5 DEFAULT DESIGN SCAN (MAINTENANCE PROCESSOR)

d) SEE FIGURE 6 DEFAULT DESIGN (MAINTENANCE PROCESSOR)

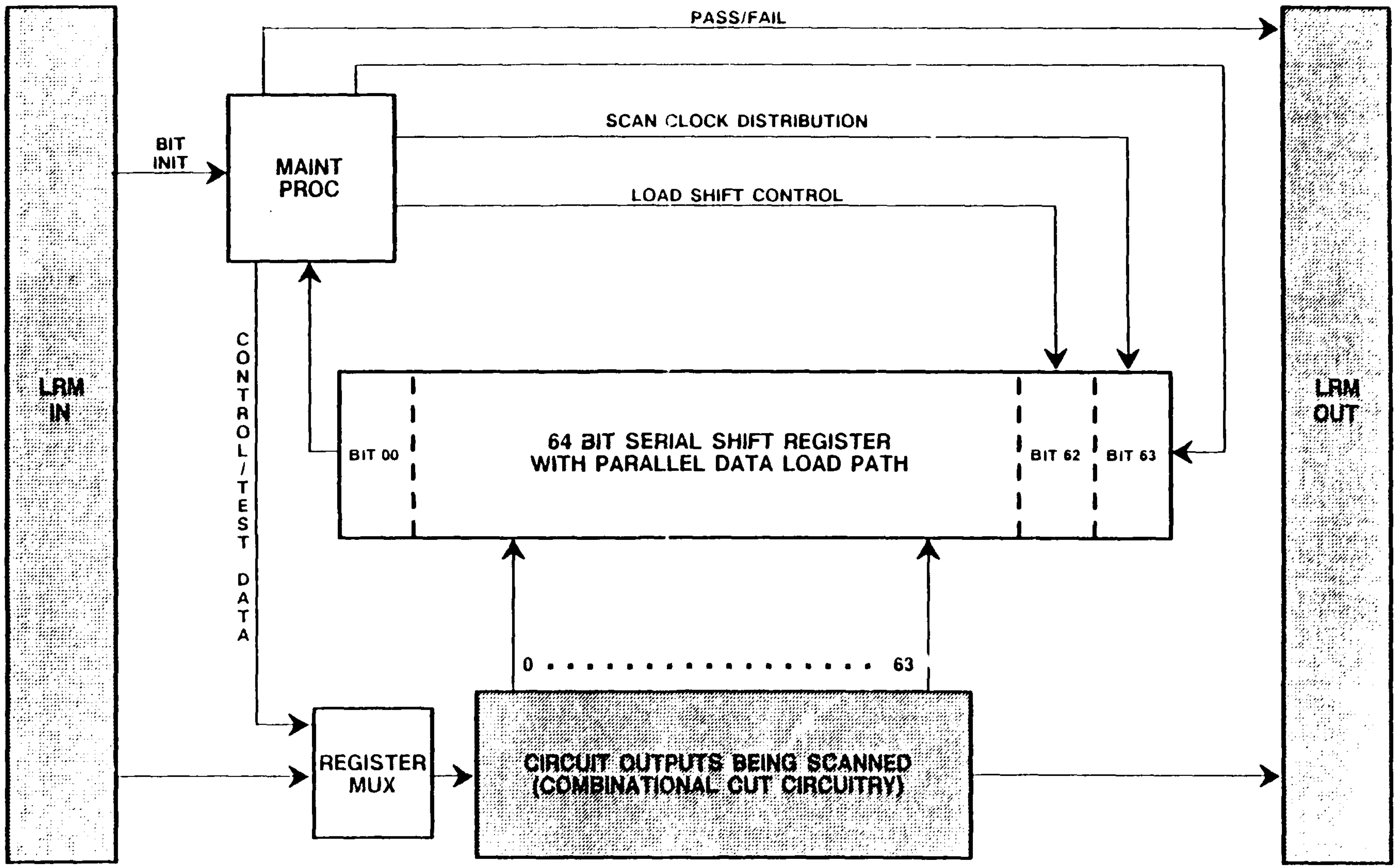
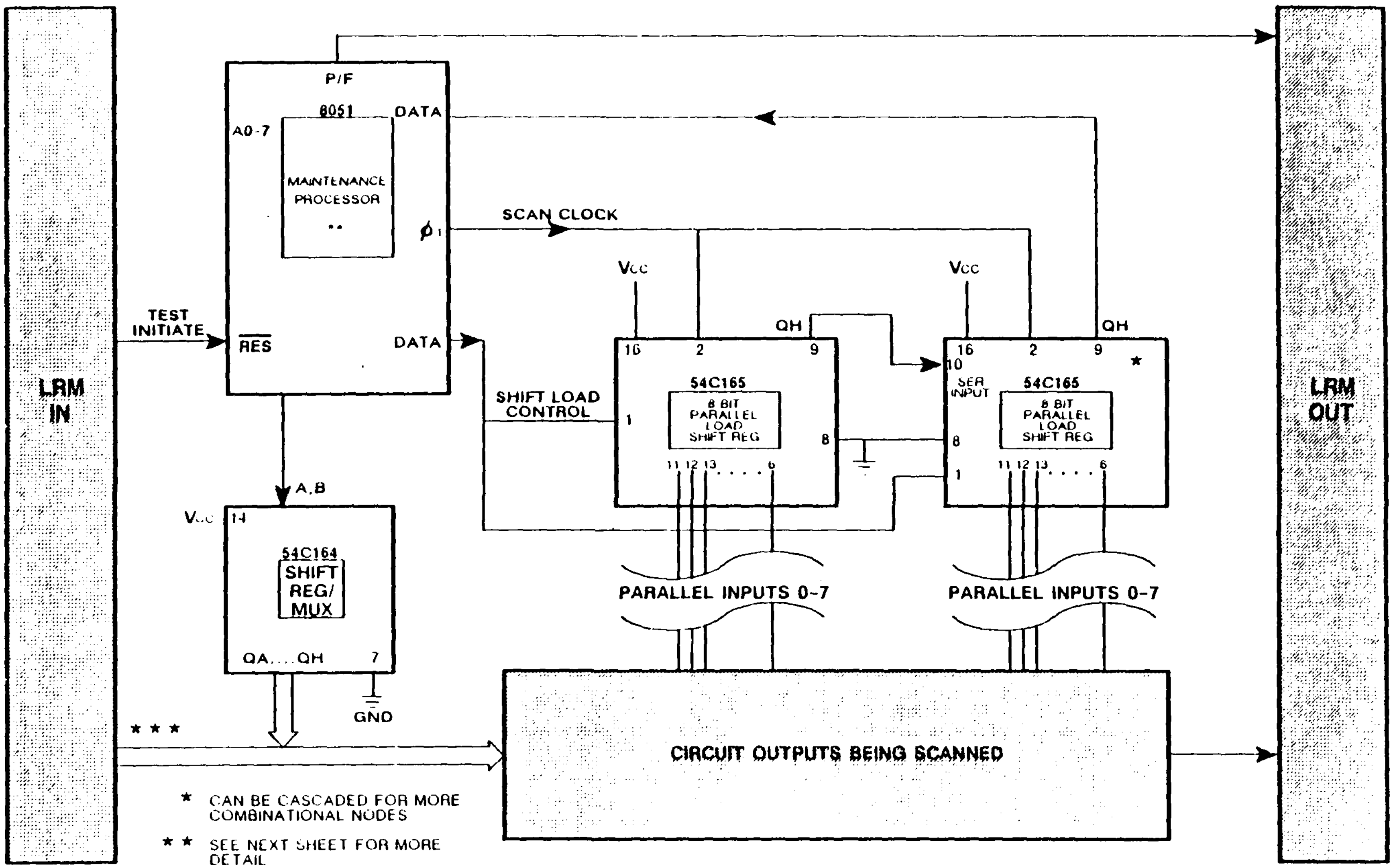


FIGURE 3 LEVEL II BLOCK DIAGRAM
SCAN BIT TECHNIQUE (SET)



* CAN BE CASCADED FOR MORE COMBINATIONAL NODES

** SEE NEXT SHEET FOR MORE DETAIL

*** CIRCUITS DRIVING PRIMARY INPUTS MUST BE IIN TRISTATE CONDITION WHEN APPLYING BIT TEST INPUT

FIGURE 4 DEFAULT DESIGN (SCAN/SET)

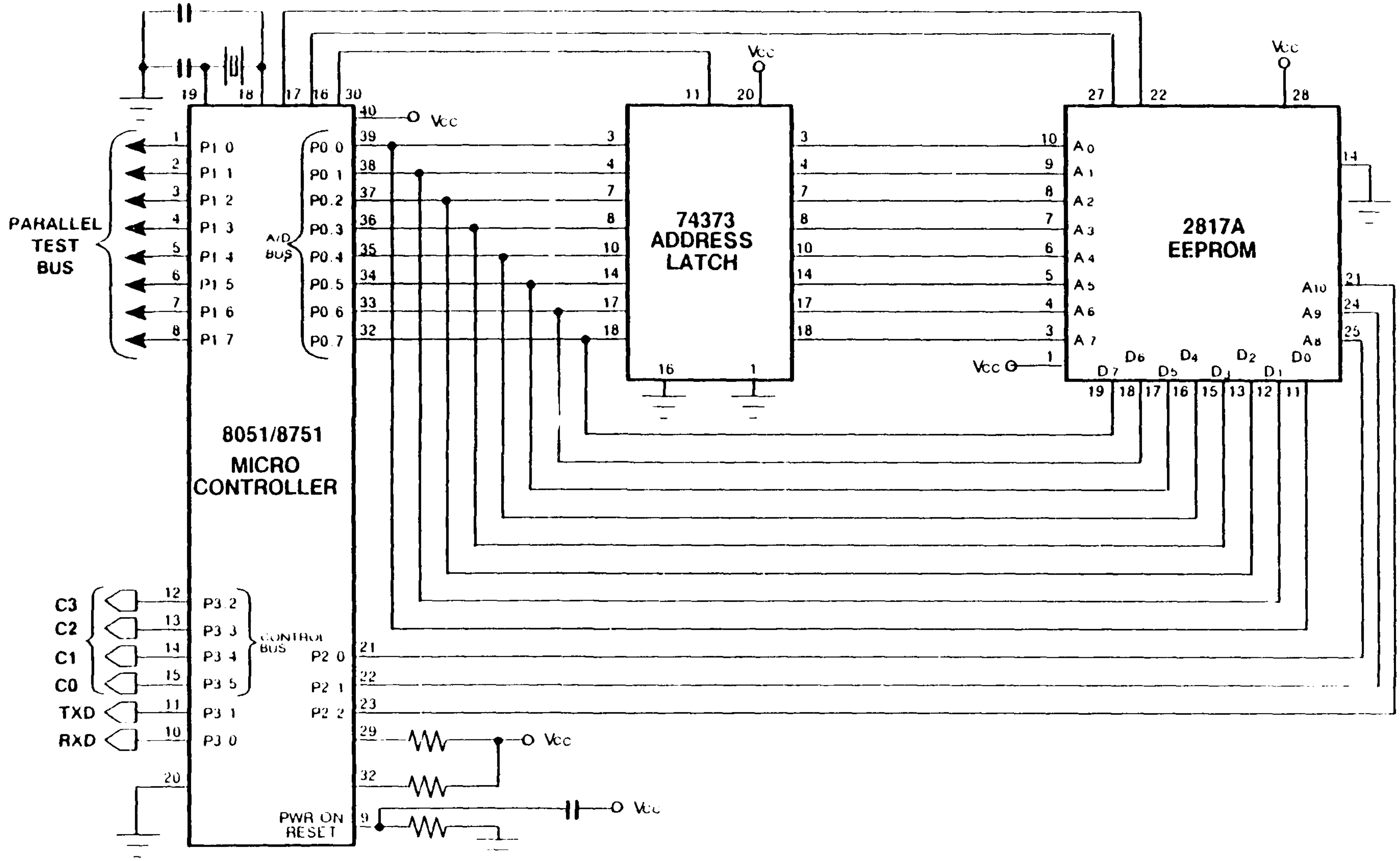
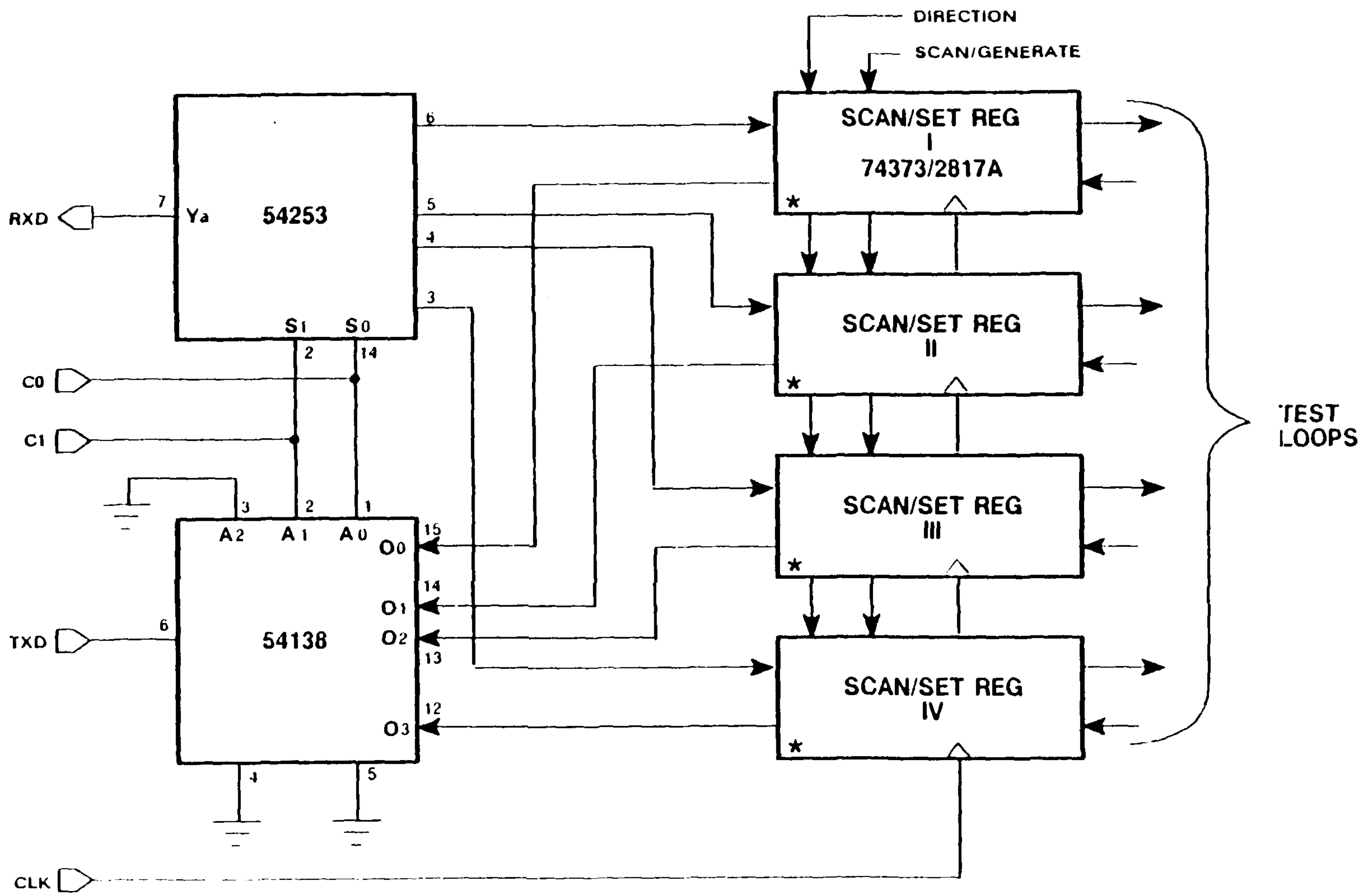


FIGURE 5 DEFAULT DESIGN SCAN
(MAINTENANCE PROCESSOR)



* DEFAULT DESIGN ON PRIOR PAGE
ONLY UTILIZES ONE LOOP

FIGURE 6 DEFAULT DESIGN
(MAINTENANCE PROCESSOR)

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES

CATEGORY: LONG TUTORIAL | **PAGE** 11 **of** 12

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

NUMBER/NAME	AREA *(sq in)*	# OF PINS	POWER TYPICAL *(mW)*	POWER MAX. *(mW)*	WEIGHT *(gms)*
8051/8751 (1)	1.20	40	175	750	2.0
2817A (1)	0.30	28	300	750	1.4
54HCT253 (1)	0.24	16	0.150	0.500	1.0
54C165	0.25	16	0.150	0.500	1.1
54C164	0.23	14	0.150	0.500	1.1
54HCT273/373	0.30	20	0.250	0.375	1.1
54138	0.80	16	100	500	1.5

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES

CATEGORY: LONG TUTORIAL

SUBCATEGORY: DEFAULT DESIGN

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

1. B. Eichelberger and T. W. Williams, "a logic Design structure for LSI Testability", fourteenth annual design Automation Conference, New Orleans, (June 1977), pp.462-467.
2. M. J. Y. Williams and J.B. Angell, "Enhancing Testability of large scale integrated circuits via test points and additional logic", IEEE vol c-22 no. 1 (Jan 1978) pp. 46-60.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES	
CATEGORY: USER REQUESTED DATA	PAGE 1 of 1
SUBCATEGORY:	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

QUESTIONS	VARIABLE ASSIGNMENTS
1. How many nodes to be scanned?	v1
2. How many CUT primary inputs are there?	v2
3. How many test patterns are needed?	v3
4. What is the scan clock rate?	v4
5. What is the scan word compare time?	v5
6. What is the initialization time?	v6
7. What is the time to load the shift register?	v7

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES	
CATEGORY: EQUATIONS	**PAGE** 1 **of** 2
SUBCATEGORY: (DATA NOT TO BE DISPLAYED)	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒	

DATA:

I) VARIABLE DEFINITIONS

$n1$ = Number of parallel load shift registers

$n2$ = Number of maintenance processors

$n3$ = Number of serial data shift register/multiplexers

$v1$ = Number of nodes to be scanned

$v2$ = Number of primary inputs

$v3$ = Number of test patterns

$v4$ = SCAN clock rate

$v5$ = SCAN word compare time

$v6$ = Initialization time

$v7$ = Time to load shift register/multiplexer

II) COMPONENT DETERMINATION EQUATIONS

$n1 = v1/8$

$n2 = 1$

$n3 = v1/8$

III) PENALTY EQUATIONS

a) AREA (sq in)

TOTAL AREA OF BIT CHIPS = $(0.25)n1 + (3.20)n2 + (0.30)n3$

TOTAL AREA OF BIT CIRCUITRY = (Area of BIT chips) + 15% FOR PC traces.

= 1.15 (Total area of BIT chips)

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: SCAN DESIGN TECHNIQUES

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

II) PENALTY EQUATIONS (CONT)

b) WEIGHT (gms)

WEIGHT OF BIT CHIPS = (0.90)n1 + (0.95)n3 + (5.5)n2

WEIGHT OF BIT CIRCUITRY = (Weight of BIT chips) + (10% For weight of solder)

= 1.1 Weight of chips

c) POWER (mW)

MAXIMUM POWER OF BIT CHIPS = (60)n1 + (65)n3 + (450)n2

d) TIME

TEST TIME = v6 + (v3)(v7 + (v1)(v4) + v5)

PARAGRAPH 6.8
DIGITAL WRAPAROUND TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND

CATEGORY: SHORT TUTORIAL

SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE

DATA TYPE: **TEXT** [X] **LIST** [ ] **TABLE** [ ] **GRAPHIC** [ ] **EQUATIONS** [ ]

DATA:

SHORT TUTORIAL
FOR
DIGITAL WRAPAROUND

Digital Wraparound is a non-concurrent Built-In-Test (BIT) technique. This technique consists of hardware and software (firmware in Read Only Memory (ROM)) and specifically requires a microprocessor, some digital output devices and some digital input devices on board as part of the Circuit Under Test (CUT).

The technique consists of adding the necessary circuitry so that upon BIT INITIATE, the digital data leaving the digital output devices can be routed to the digital input device on the Line Replaceable Module (LRM). An appropriate BIT routine is stored in ROM along with test data to control the data transfer and compare the data received with the data transmitted. A mismatch will indicate a failure.

There are various options open to the engineer as how to route the signal back to the microprocessor. One way is to add digital gates to wrap the inputs around the outputs. Another method would be to use tristate drivers, if the digital Input/Output (I/O) is bidirectional. In this instance, no additional hardware would be required.

The Microprocessor Bit technique (a related BIT technique), checks out the internal components of the microprocessor system. The wraparound BIT can be used to extend the microprocessor BIT to include the I/O.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND

CATEGORY: SHORT TUTORIAL

SUBCATEGORY: 1. LEVEL I BLOCK DIAGRAM
2. BIT SEQUENCE FLOW CHART

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2

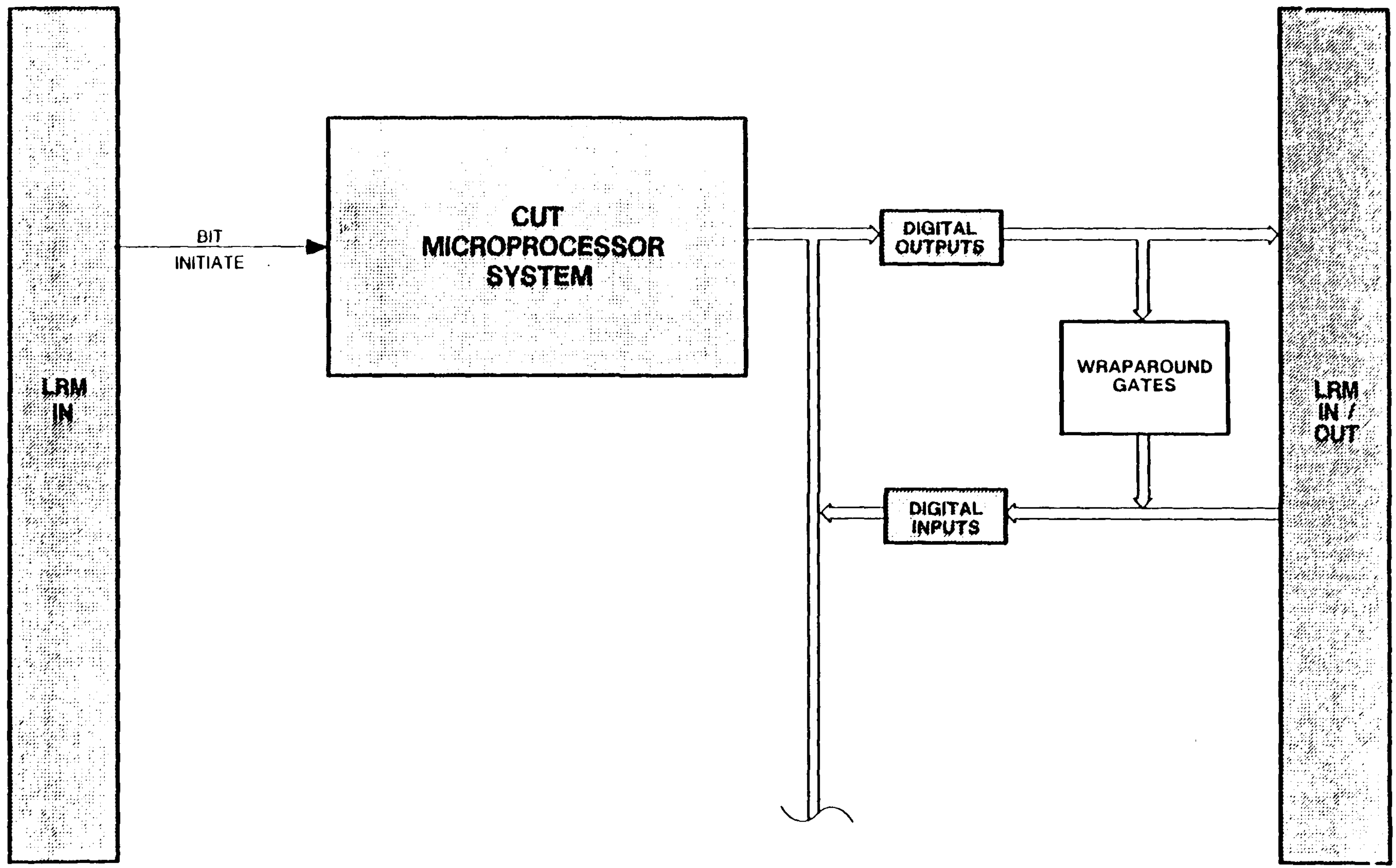


FIGURE 1 LEVEL I BLOCK DIAGRAM
DIGITAL WRAPAROUND AS A BIT TECHNIQUE

PAGE 3 of 4

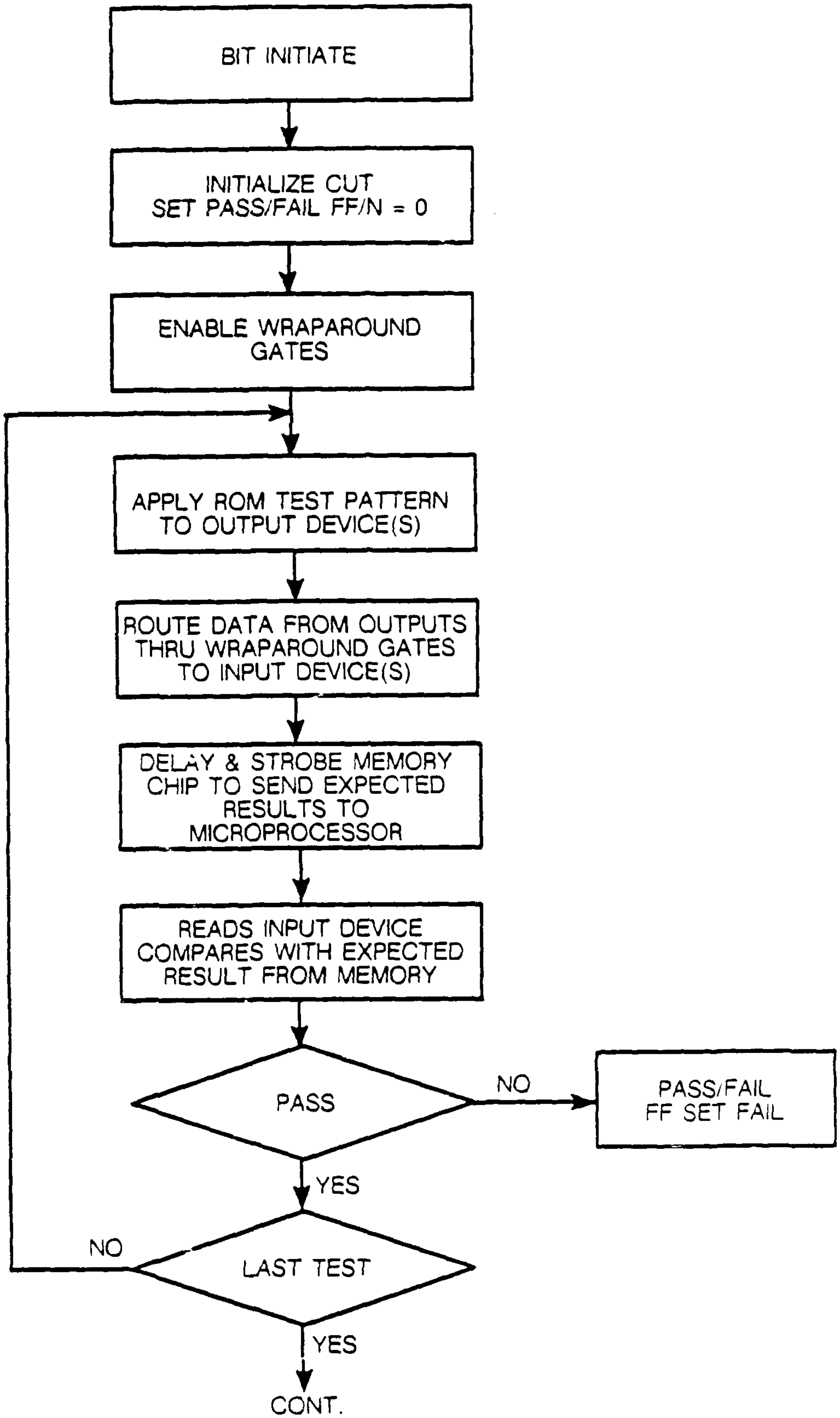


FIGURE 2 BIT SEQUENCE FLOW CHART FOR DIGITAL WRAPAROUND

PAGE 4 of 4

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
DIGITAL WRAPAROUND

1. A 'BIT INITIATE' signal is input to the LRM, so testing can begin.
2. Initialize the Circuit Under Test and set the Pass/Fail Flip-Flop to Pass.
3. Before applying a signal, enable the wraparound gates that are going to be used for that particular test.
4. Apply the ROM test patterns to the output device(s).
5. At this point, the data is routed from the outputs through the proper enabled wraparound gates and into the input device(s).
6. Delay and strobe the memory chip to send the expected results to the microprocessor.
7. Microprocessor reads the results from the input device(s) and compares it with expected result from memory.
8. If comparison fails, set Pass/Fail Flip-Flop to FAIL and end test. If comparison passes, continue.
9. If not the last ROM address, go back to STEP 4 and continue.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

DIGITAL WRAPAROUND
ADVANTAGES

1. Only requires minimal hardware and is a conceptually simple design which is easy to implement.

2. Chips that are needed are readily available (the wraparound device is generally standard gates of the same logic family used in the digital I/O).

3. This technique may also be used in conjunction with "MICROPROCESSOR BIT", another Computer Aided Design Built-In Test Technique (CAD-BIT TECHNIQUE), to extend the BIT coverage to include the I/O chips (which are not normally checked out with the microprocessor BIT).

4. If the digital interface is bidirectional, no additional hardware will be required.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE DISADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

DIGITAL WRAPAROUND
DISADVANTAGES

1. This technique only checks out a small portion of the LRM

2. If the number of test patterns needed to completely test the digital I/O is large (for example - a MIL-STD 1553 interface), then additional ROMs may have to be added to store the test patterns. This will increase the real estate penalty. However, if the I/O devices are simply buffers, only a few patterns will be required and most ROMs will have spare locations.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

DIGITAL WRAPAROUND
ATTRIBUTES

1. REAL ESTATE PENALTY
   - SMALL - Basically requires several integrated circuit packages of gates
   - ROMs - Depends on number of test patterns (as patterns increase, any spare ROM, locations may be depleted, therefore an additional ROM(s) may have to be added)
   - If number of I/O lines are large, there will be a corresponding increase in number of wraparound gates required
2. POWER PENALTY
   - Small - Just requires additional power to wraparound gates and additional ROM if needed
3. RELIABILITY PENALTY
   - Minimal impact since only a few gates of the same logic family as the I/O devices are added
4. TIMING PENALTY
   - Number of test patterns multiplied by the pattern application rate
5. NON-CONCURRENT
6. CONCEPTUAL COMPLEXITY
   - Straight forward

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

DIGITAL WRAPAROUND
ATTRIBUTES
(CONT)

7. HARDWARE/SOFTWARE/COMBO
   - Hardware present/test patterns in firmware
8. TECHNOLOGY
   - All current digital technologies
9. IS BITE SELF TESTABLE?
   - No
10. DESIGN COST
    - Will be kept at a minimum since the chips needed are readily available
    - The microprocessor used can also be used for other BIT techniques
    - Engineering time to create patterns depends on complexity of I/O chips to be tested

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND	
CATEGORY: LONG TUTORIAL	**PAGE** 6 **of** 11
SUBCATEGORY: DEFAULT DESIGN	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

a) SEE FIGURE 3 FOR DIGITAL WRAPAROUND BIT TECHNIQUE LEVEL II BLOCK DIAGRAM - UTILIZING DIGITAL WRAPAROUND

b) SEE FIGURE 4 FOR DIGITAL WRAPAROUND BIT TECHNIQUE DEFAULT DESIGN

c) SEE FIGURE 5 FOR DIGITAL WRAPAROUND TECHNIQUE DEFAULT DESIGN

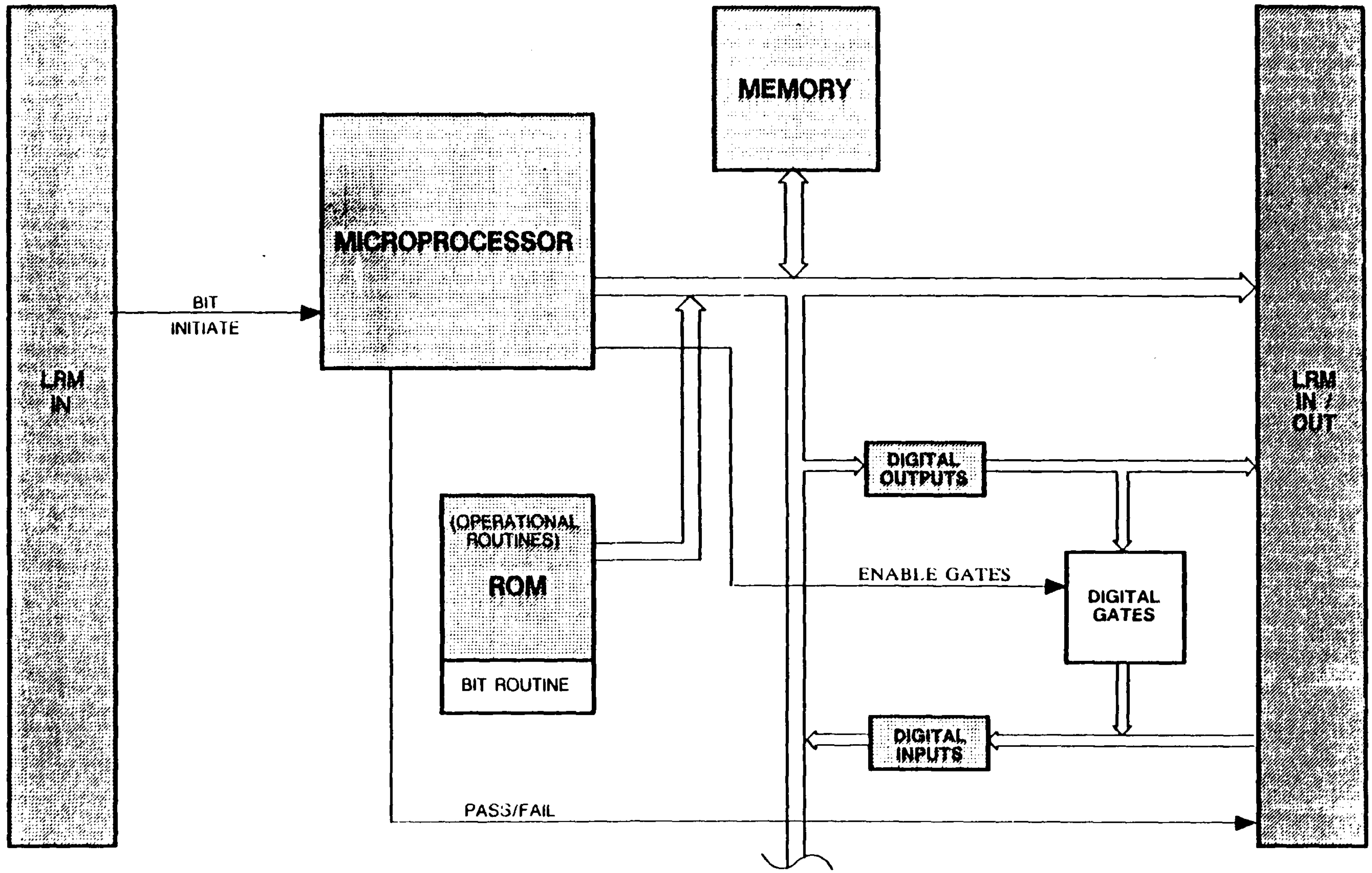


FIGURE 3 LEVEL II BLOCK DIAGRAM UTILIZING DIGITAL WRAPAROUND

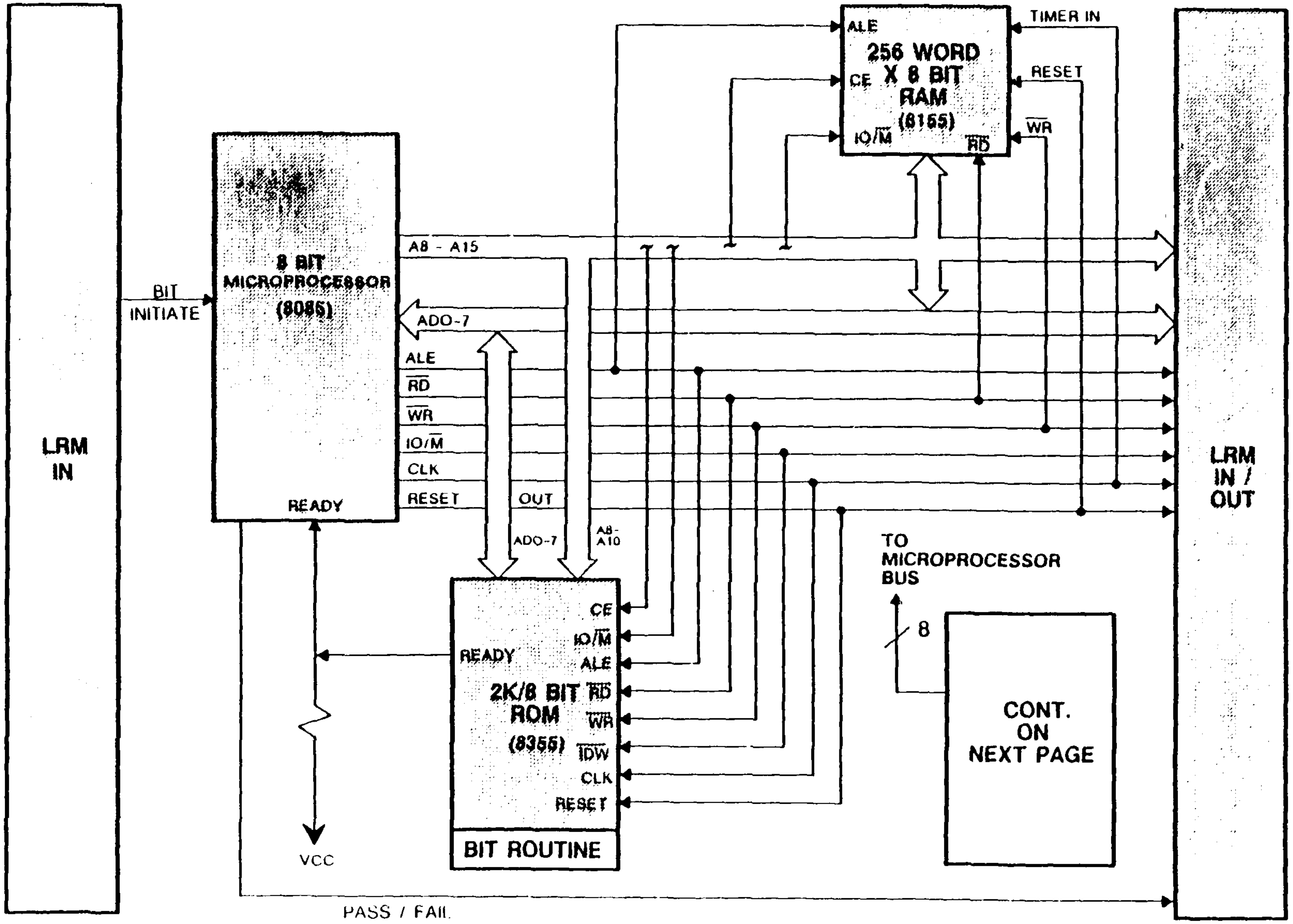


FIGURE 4 DEFAULT DESIGN – DIGITAL WRAPAROUND

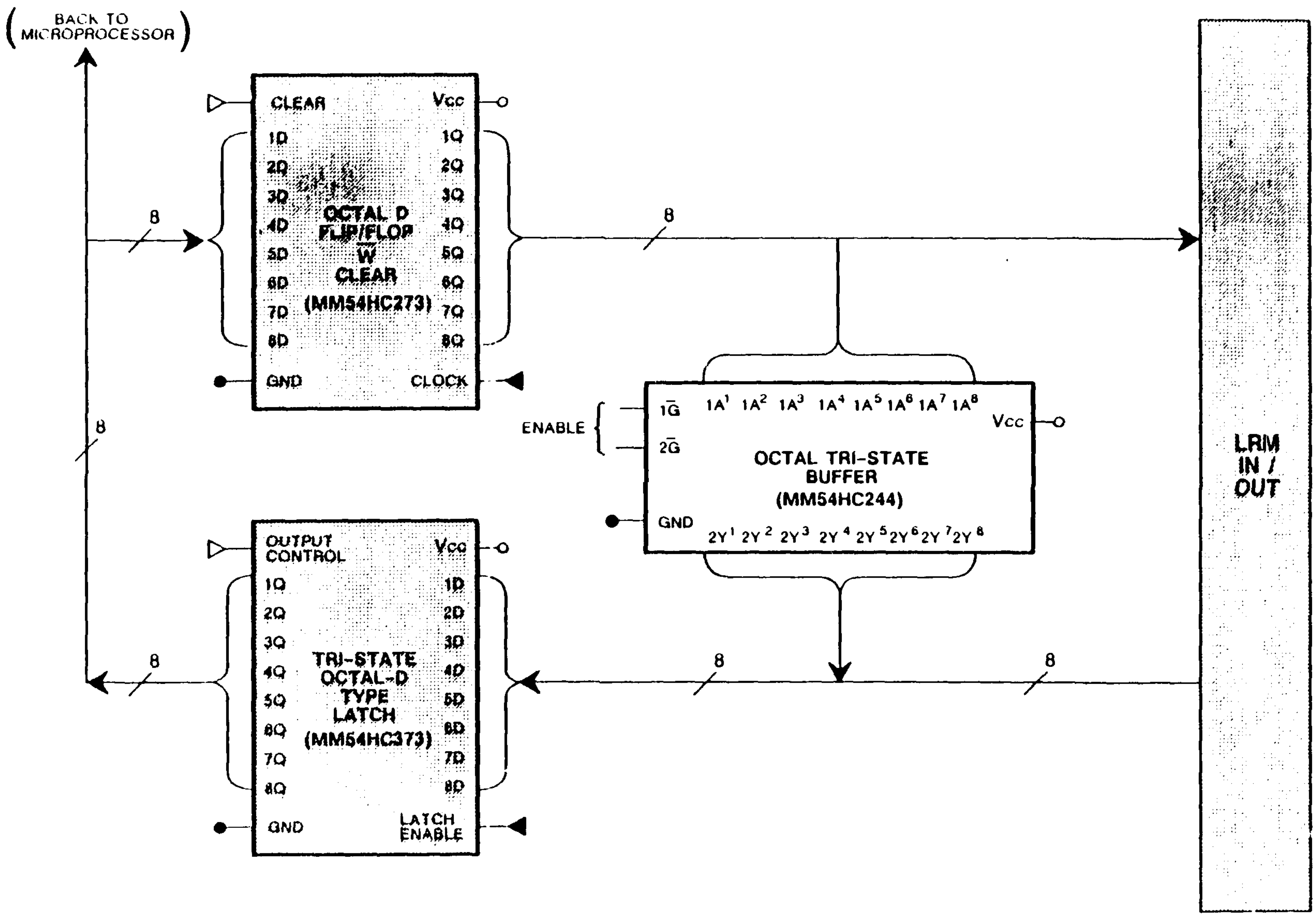


FIGURE 5 DEFAULT DESIGN – DIGITAL WRAPAROUND

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND

CATEGORY: LONG TUTORIAL

SUBCATEGORY: PARTS DATA LIST

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

NUMBER/NAME	AREA SQ. IN	# OF PINS	POWER TYPICAL *(mW)*	POWER MAX. *(mW)*	WEIGHT *(gms)*
OCTAL TRI-STATE BUFFER (MM54HC244)	0.2167	20	350	500	3.3

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND	
CATEGORY: LONG TUTORIAL	PAGE 11 of 11
SUBCATEGORY: BIBLIOGRAPHY	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

NONE REQUIRED

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND	
CATEGORY: USER REQUESTED DATA	**PAGE** 1 **of** 1
SUBCATEGORY:	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

QUESTIONS	VARIABLE ASSIGNMENTS
1. How many digital outputs are to be wrapped around?	v1
2. How many test patterns are required to be stored in ROMs (bytes)?	v2
3. What is the test pattern application rate (bytes/sec)?	v3
4. What is the initialization time?	v4

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND

CATEGORY: EQUATIONS | **PAGE** 1 **of** 2

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITION

n1 = Number of wraparound gate chips

v1 = Number of digital outputs to be wrapped around

v2 = Number of test patterns stored in ROM

v3 = Test pattern application rate (bytes/sec)

v4 = Initialization time (sec)

II) COMPONENT DETERMINATION EQUATIONS

n1 = v1/8

III) PENALTY EQUATIONS

a) AREA (sq in)

AREA of BIT CHIPS = (0.2167)n1

TOTAL AREA of BIT CIRCUITRY = (Total area of chips) + 15% for PC traces
= 1.15 (Area of BIT Chips)

b) WEIGHT (gms)

WEIGHT OF BIT CHIPS: = (6.5)n1

WEIGHT OF BIT CIRCUITRY = Weight of BIT chips + 10% Weight of solder
= 11.0 (Weight of chips)

c) POWER (mw)

MAXIMUM POWER: = (350)n1

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: DIGITAL WRAPAROUND

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

d) TEST TIME

TEST TIME = (v2)(v3) + v4

PARAGRAPH 6.9

PSEUDO RANDOM PATTERN GENERATOR WITH MULTIPLE INPUT SHIFT REGISTER (PRPG/MISR) TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)	
CATEGORY: SHORT TUTORIAL	**PAGE** 1 **of** 4
SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE	

DATA TYPE: TEXT [x] LIST [ ] TABLE [ ] GRAPHIC [ ] EQUATIONS [ ]

DATA:

SHORT TUTORIAL
FOR
PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE
INPUT SHIFT REGISTER (MISR)

This non-concurrent self test method can be implemented in hardware without requiring numerous test patterns or good machine responses to be stored internally. Testing begins upon activation of a test initiate signal, after which the test control logic initializes the Pseudo Random Pattern Generator (PRPG) which then generates and applies a set of pseudo random test patterns to the Circuit Under Test (CUT) by multiplexing out the primary inputs and multiplexing in the PRPG outputs. A PRPG with n outputs will pseudo randomly cycle through all but one possible n - bit binary patterns, which sums up to $2^n - 1$ possible bit patterns. In order to determine if the CUT's response to these patterns are correct, the outputs of the CUT are connected in parallel to the Multiple Input (linear feedback) Shift Register (MISR) which compresses the test result data into a single m - bit signature. If the test result signature identically compares to the good machine signature, the test passes. This test method is advantageous because one achieves a substantial amount of testing with a relatively small amount of hardware. The amount of hardware can even be further reduced by modifying a few choice flip-flops required in the CUT and converting them to dual purpose, test/function flip-flops.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)

CATEGORY: SHORT TUTORIAL

SUBCATEGORY:
1. LEVEL I BLOCK DIAGRAM
2. BIT SEQUENCE FLOW CHART

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2

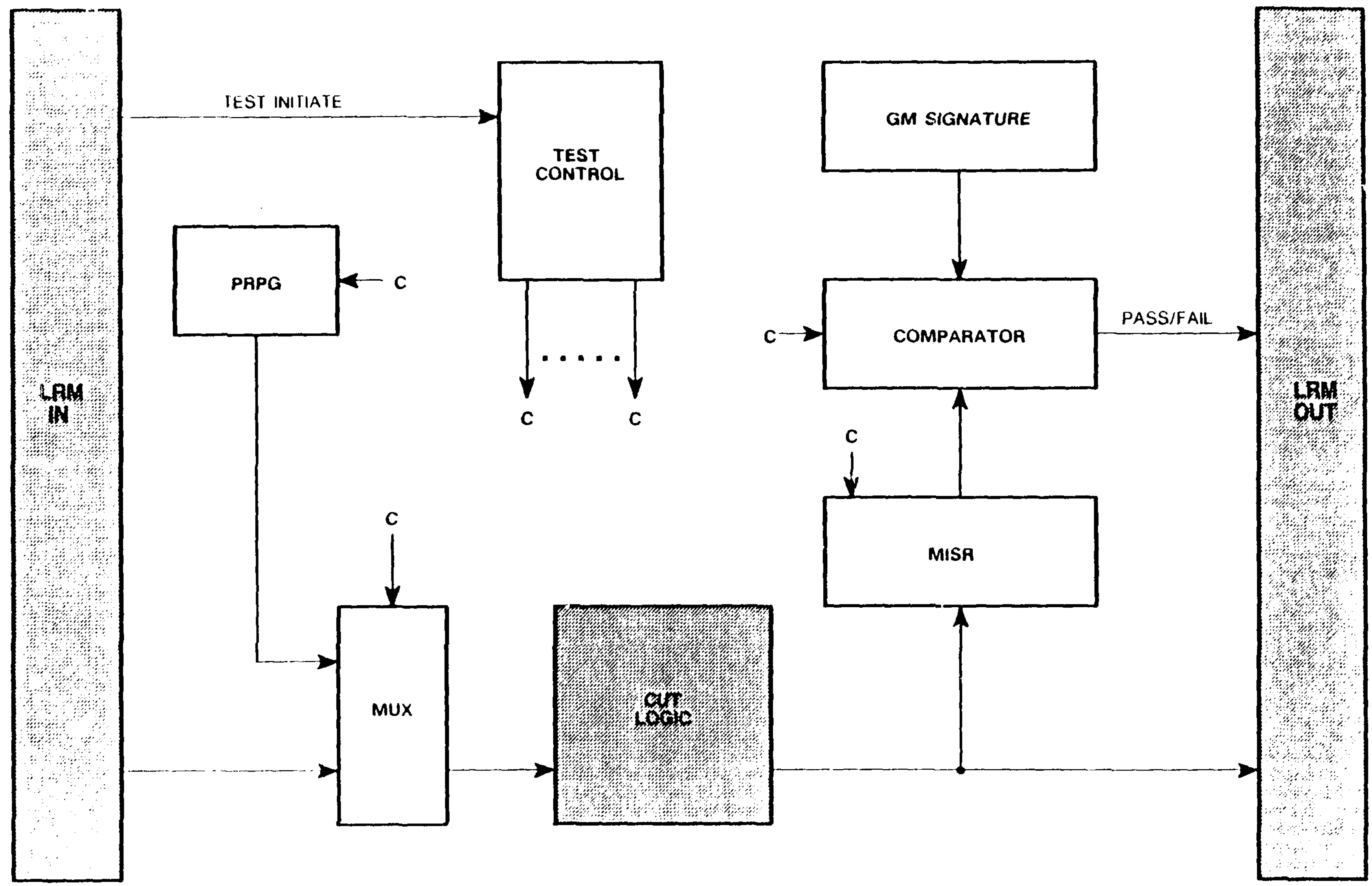


FIGURE 1 LEVEL I BLOCK DIAGRAM
PRPG/MISR

PAGE 3 of 4

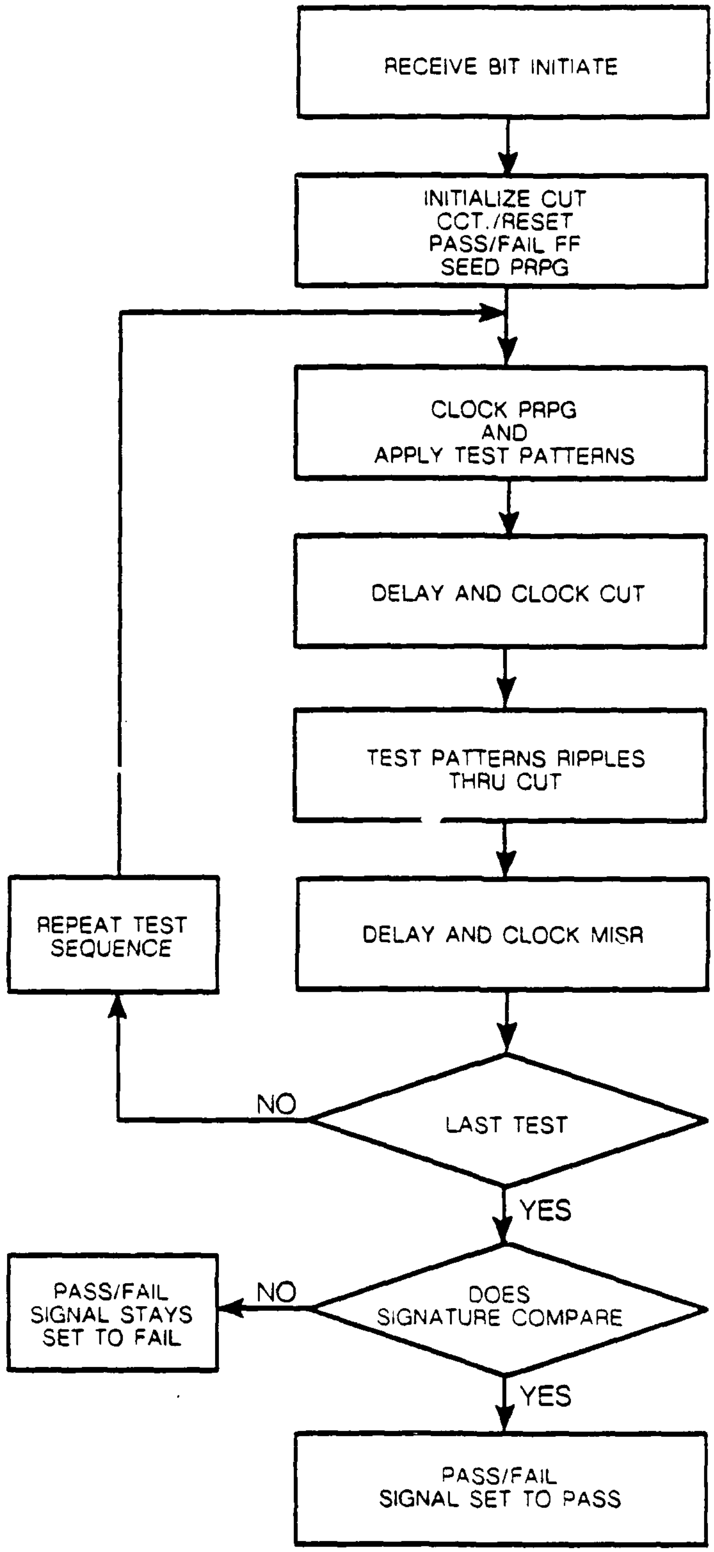


FIGURE 2 BIT SEQUENCE FLOW CHART
FOR PRPG/MISR BIT

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE
INPUT SHIFT REGISTER (MISR)

1. Receive BIT initiate and start test.

2. Initialize UUT, reset circuits, seed PRPG.

3. Clock Pseudo Random Pattern Generator and apply test patterns.

4. Delay and clock CUT, test patterns ripple through CUT.

5. Delay and clock multiple input shift register.

6. Repeat test sequence until all patterns are sent.

7. Compare signature with response, set pass/fail.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)	
CATEGORY: LONG TUTORIAL	**PAGE** 2 **of** 13
SUBCATEGORY: BIT TECHNIQUE ADVANTAGES	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE
INPUT SHIFT REGISTER (MISR)
ADVANTAGES

1. PRPG/MISR is a very cost effective BIT due to the fact that large amounts of test patterns that can be generated without large amounts of hardware.

2 No software overhead.

3. Multiple input shift registers allow many CUT outputs to be tested at once.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)	
CATEGORY: LONG TUTORIAL	**PAGE** 3 **of** 13
SUBCATEGORY: BIT TECHNIQUE DISADVANTAGES	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR) DISADVANTAGES

1. A PRPG can not fully generate specific pairs of test patterns that must occur in sequence in order to detect faults in certain sequential logic designs.

2. More psuedo random patterns may be required to achieve a desired level of fault detection than a set of test vectors which can be individually defined such as in the ON-BOARD ROM technique.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR) ATTRIBUTES

1) REAL ESTATE PENALTY
   - Real Estate penalty will be small because all of the test patterns are generated by a single shift register and all of the CUT response are accumulated in a single register.

2) POWER PENALTY
   - Power penalty will be small since real estate penalty is small and bit chips use same type of chip as CUT.

3) RELIABILITY PENALTY
   - Slight decrease of reliability due to addition of a small number of register chips. Becomes negligible for very large combinational CUT circuitry.

4) TIMING PENALTY
   - Slight increase in processing time - 80 nsec typical Transistor Transistor Logic (TTL).

5) NON CONCURRENT

6) CONCEPTUAL COMPLEXITY - straight forward.

7) HARDWARE/SOFTWARE/COMBO
   - Hardware

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE
INPUT SHIFT REGISTER (MISR)
ATTRIBUTES
(CONT)

8) TECHNOLOGY
   - All current technologies

9) IS BITE SELF TESTABLE?
   - PRPG can be sent into MISR and read out.

10) DESIGN COST
   - Minimal with off the shelf chips available.

11) STAND-ALONE (SELF CONTAINED BIT?)
   - Yes

12) WEIGHT PENALTY
   - Roughly proportional to real estate penalty.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)	
CATEGORY: LONG TUTORIAL	**PAGE** 6 **of** 13
SUBCATEGORY: DEFAULT DESIGN	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

a) SEE FIGURE 3 FOR PRPG/MISR LEVEL II BLOCK DIAGRAM

b) SEE FIGURE 4 FOR PRPG/MISR DEFAULT DESIGN

c) SEE FIGURE 5 FOR 8 INPUT MISR CONCATENATED BUILDING BLOCKS

d) SEE FIGURE 6 FOR PRPG/MISR BIT TEST CONTROL LOGIC

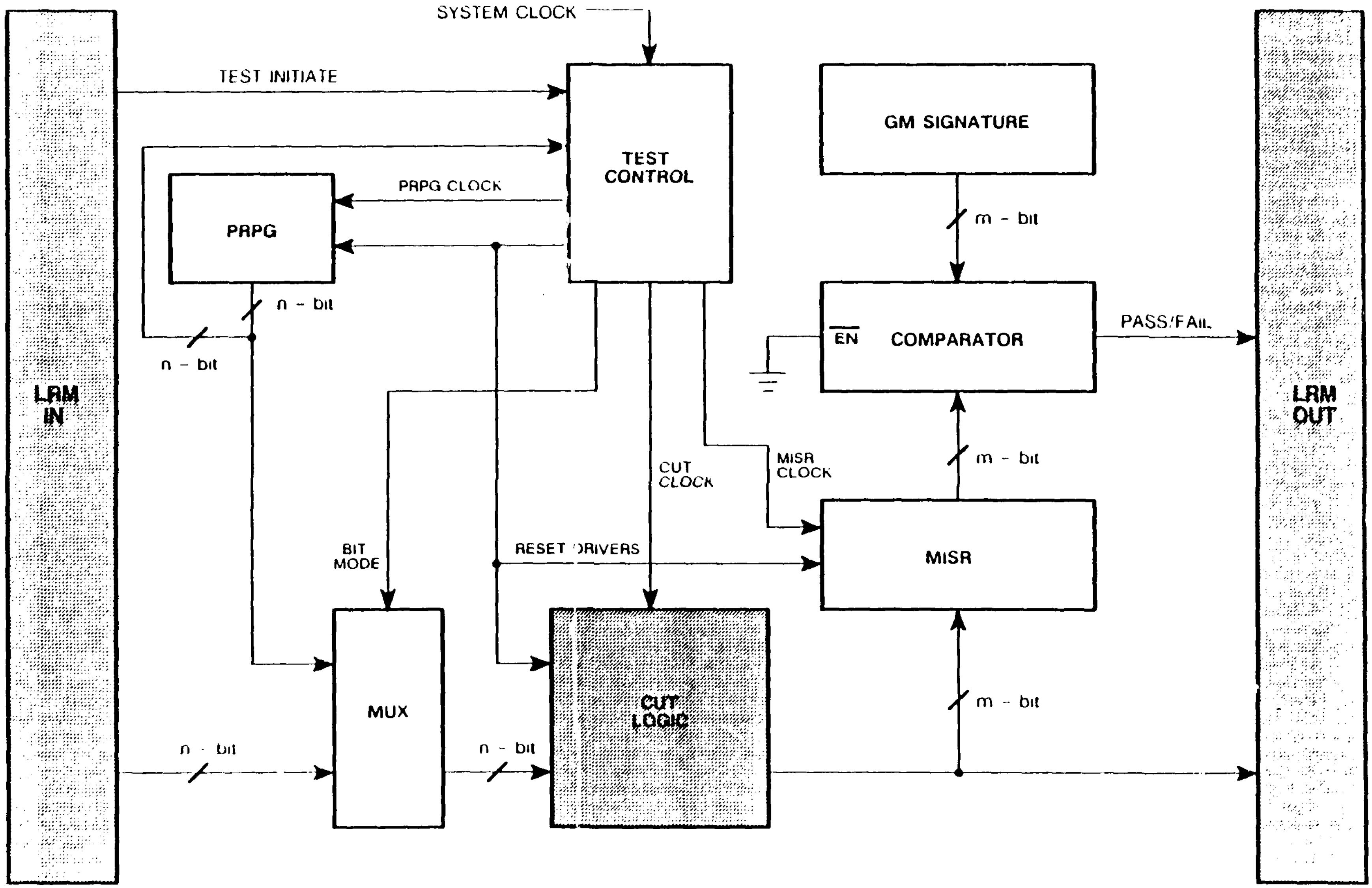
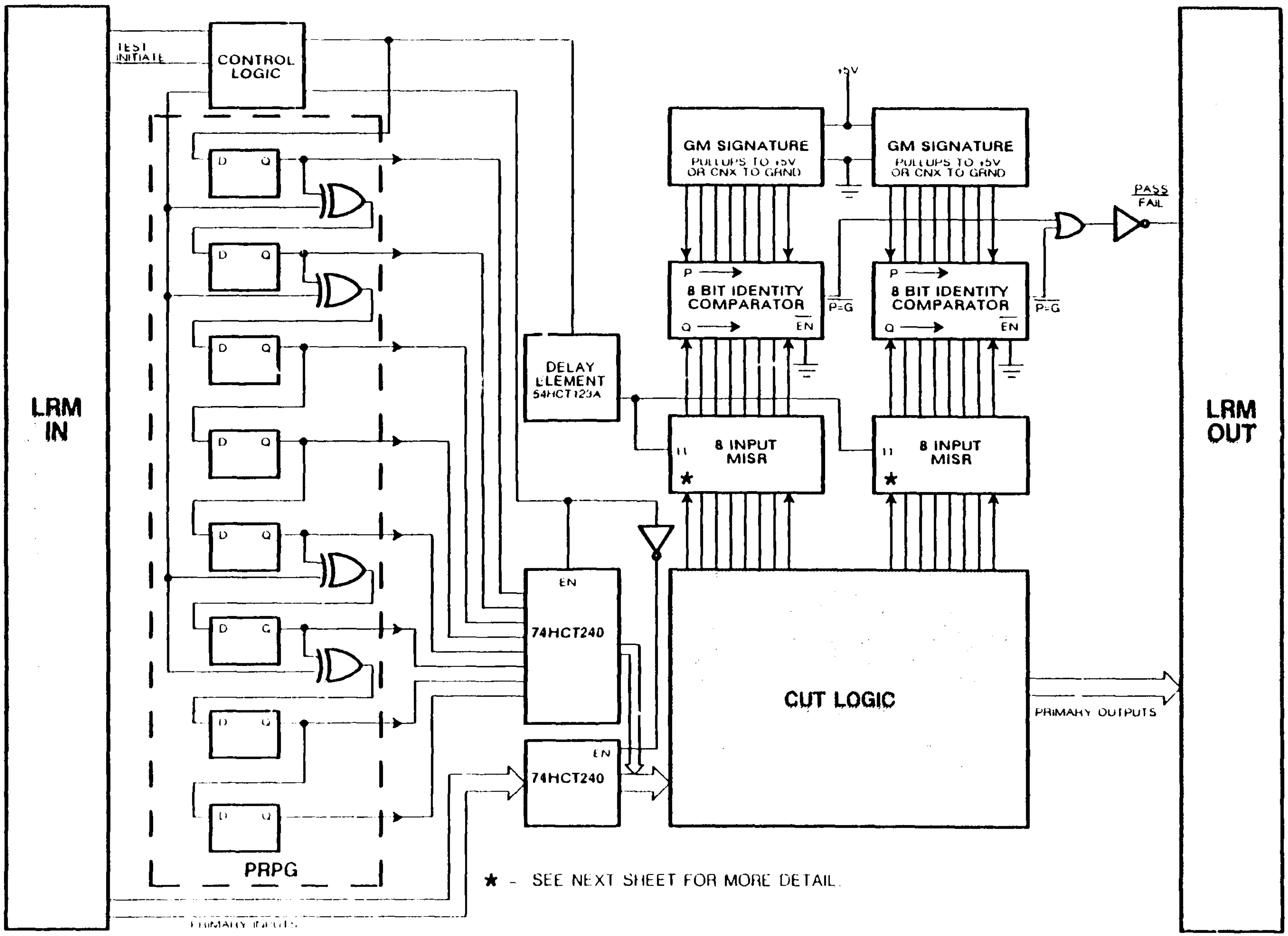


FIGURE 3 LEVEL II BLOCK DIAGRAM
PRPG/MISR



★ - SEE NEXT SHEET FOR MORE DETAIL.

FIGURE 4 DEFAULT DESIGN PRPG/MISR

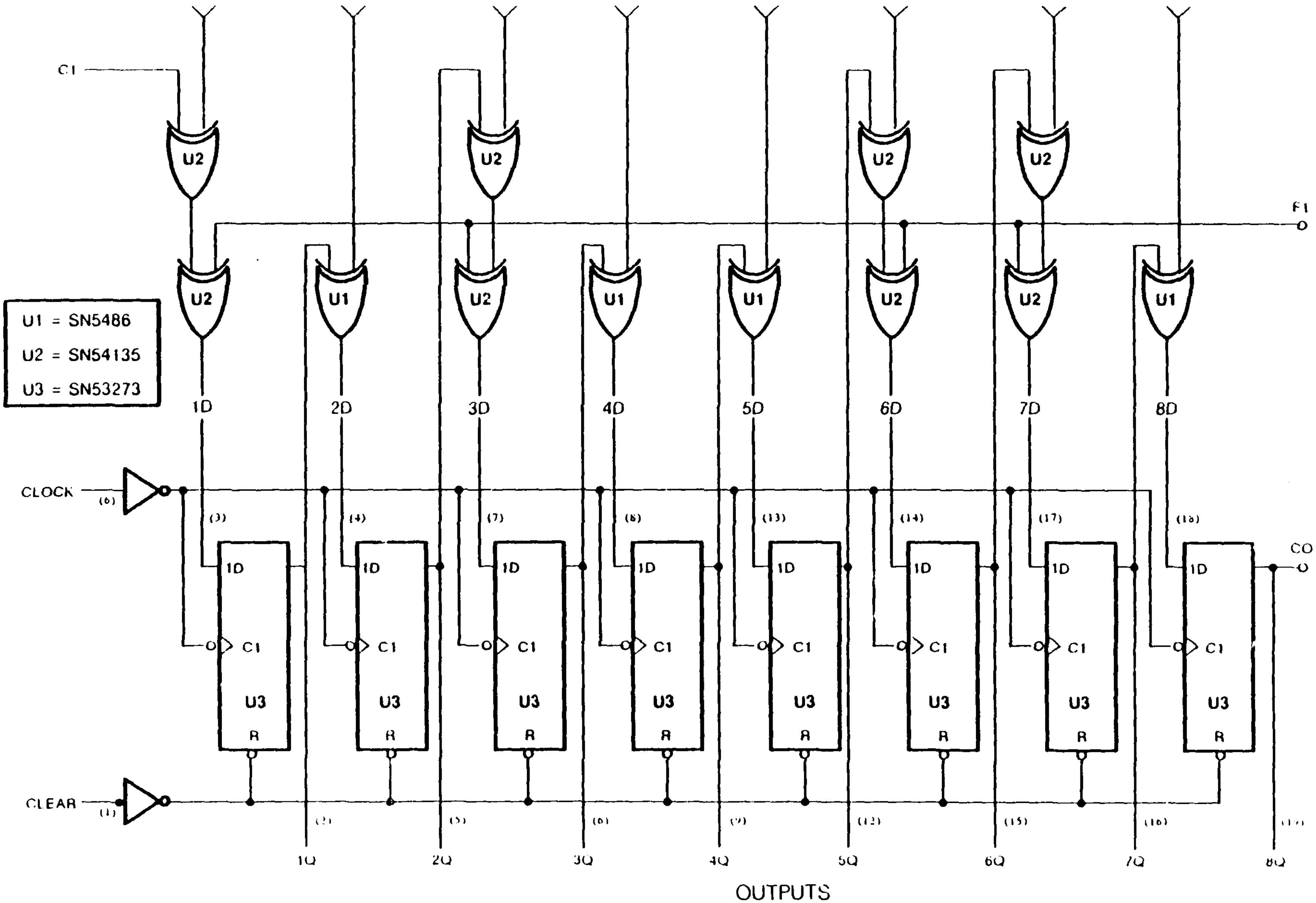


FIGURE 5 8 INPUT MISR [CONCATENATED BUILDING BLOCKS]

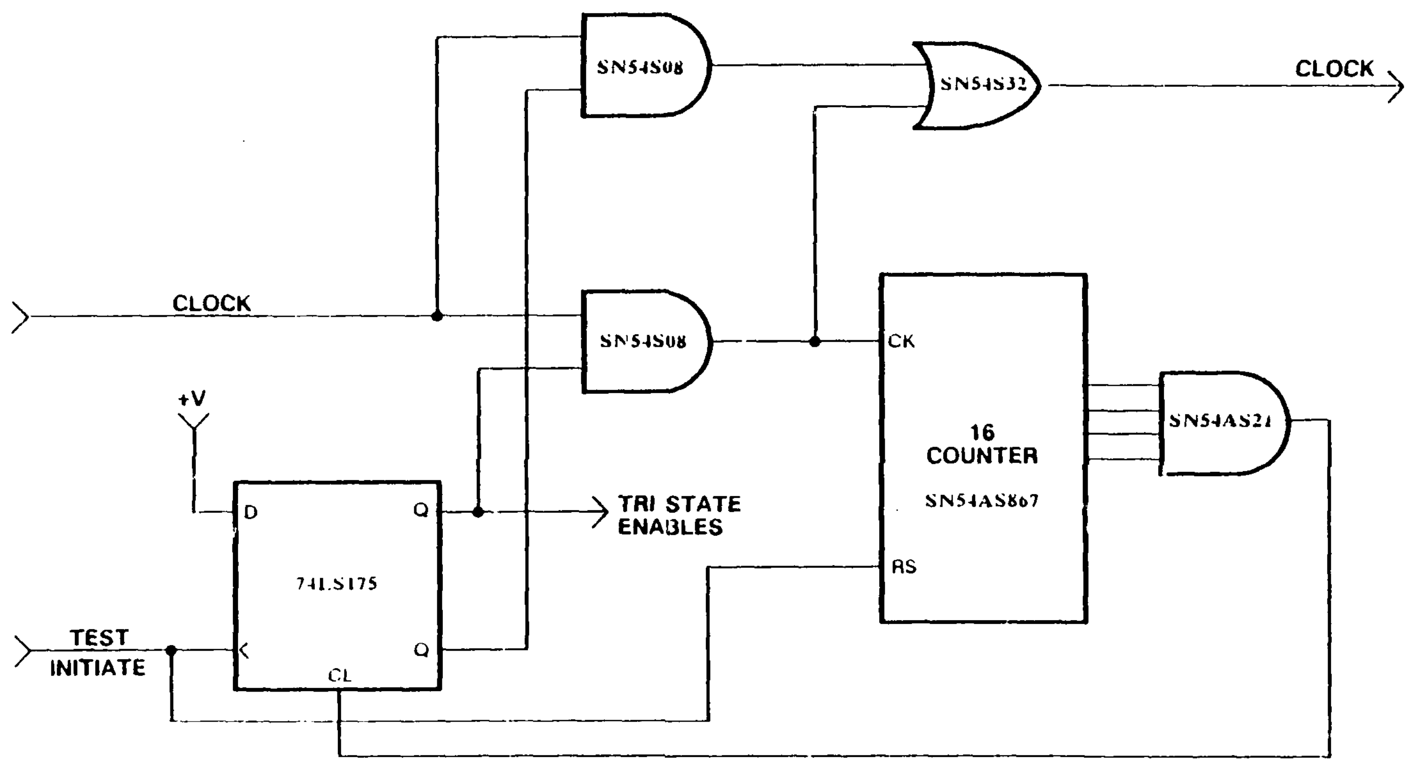


FIGURE 6 TEST CONTROL LOGIC FOR PRPG/MISR BIT

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)

CATEGORY: LONG TUTORIAL

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

NUMBER/NAME	AREA (sq in)	# OF PINS	POWER TYPICAL (mW)	POWER MAX. (mW)	WEIGHT (gms)
74LS175/ D FLIP FLOP	0.20	16	60	90	0.9
SN54AS08/ AND CHIP	0.24	14	260	440	1.1
SN54A21/ AND CHIP	0.23	14	300	540	1.1
SN54AS32/ OR CHIP	0.23	14	300	540	1.1
SN54AS8851/ COMPARATOR	0.37	24	50	85	1.6
SN54AS867/ 8 BIT COUNTER	0.37	24	44	126	1.6
74HCT240/ TRI-STATE	0.30	14	100	150	1.2
54HCT123/ DELAY ELEMENT	0.31	14	50	85	[illegible]
* R (PULLUPS)	0.30			250	0.2

* RESISTORS MAY BE USED FOR GM SIGNATURES. IN MOST CASES THEY WILL BE 1/4 1/4 WATT 5% TOL

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)

CATEGORY: LONG TUTORIAL

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

MISR

IC INFO	IC-IC PIN NUMBERS			IC-OUTSIDE PIN NUMBERS		
FUNCTION/NAME	TED-SR	EO-SR	EO-TED	PIN CALLOUTS	D-IN	D-OUT
SHIFT/REGISTER SN54273 (SR)	(3-18)	(14-3) (1-19)		CI=TEO-1 CLR=SR-1	TEO-2 EO-2 TEO-5 EO-5 EO-9 TEO-11 TEO-14 EO-13	SR- 19 16 15 12 9 6 5 2
EXCLUSIVE-OR SN5486 (EO)	(7-14) (6-16)	(3-17) (4-15)	(4-12)	CO=SR-2		
TRI-INPUT EX-OR (TEO) SN54135	(10-9) (9-7) (13-4) (15-6)	(6-13) (8-12) (10-8) (12-5)		CLK=SR-11 FI= TEO-(4-12)		

PRPG

	EO-SR	EO-EO	SR-SR			
SHIFT/REGISTER SN54273 (SR)	(3-18) (6-14)	(2-5-9-13)	(19-17) (15-13)	CI=EO-1 CLR=SR-1 CO=SR-2		SR- 19 16
EXCLUSIVE-OR SN5486 (EO)	(10-7) (11-4) (4-16) (8-9) (12-6)		(12-8) (5-3)	CLK=SR-11 FI= EO(2-5-9-12)		15 12 9 6 5 2

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIBLIOGRAPHY

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BILBO - Built-In Logic Block Observation Techniques
79 - Koenemann, Mucha, Zwieoff - 1979 IEEE Test Conference

81 - Segers - 1981 IEEE Test Conference -
A Self-Test Method for Digital Circuits

STUMPS - Self Testing of Multi Chip Logic Modules
82 - Bardell, McAnney - 1982 IEEE Test Conference

83 - Komonytsky - Electronics 1983 -
Synthesis of techniques creates complete system self-test

84 Butt, El-ziq - 1984 International Test Conference - Impact of Mixed-Mode Self-Test On Life Cycle Cost Of VLSI Based Designs

84 - LeBlanc - 1984 IEEE Design & Test of Computers -
LOCST: A Built-In Self-Test Technique

85 - Bhavsar - 1985 International Test Conference -
"Concatenable Polydividers": BIT-Sliced LFSR Chips For Board Self-Test

86 - Sabo, Johannsen, Yau - 1986 Custom Integrated Circuits Conference - Genesil Silicon Compilation and Design for Testability

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)

CATEGORY: USER REQUESTED DATA **PAGE** 1 **of** 1

SUBCATEGORY:

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

QUESTIONS	VARIABLE ASSIGNMENT
1. How many primary input pins are used by the LRM's operational circuitry?	v1
2. How many primary output pins are used by the LRM's operational circuitry?	v2
3. What is the number of tests patterns?	v3
4. What is the system clock period?	v4
5. What is the estimated initialization time?	v5

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)

CATEGORY: EQUATIONS | **PAGE** 1 **of** 2

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITION

n1 = Number of PRPG registers

n2 = Number of MISR registers

n3 = Number of test control logic modules

v1 = Number of CUT inputs

v2 = Number of CUT outputs

v3 = Number of test patterns

v4 = CUT clock speed

v5 = Time for initialization

II) COMPONENT DETERMINATION EQUATIONS

n1 = v1/8

n2 = v2/8

n3 = 1

III) PENALTY EQUATIONS

a) AREA (sq in)

Area of BIT chips = (1.79)n1 + (1.163)n2 + n3 + (0.65)n3

Total area of BIT circuitry = (Area of BIT chips) + 15% For PC traces

= 1.15 (Area of BIT chips)

b) WEIGHT (gms)

Weight of BIT chips = (21)n1 + (15.5)n2 + (14)n3

Total weight of BIT circuitry = (Weight of BIT chips) + 10% For weight of solder

= 1.15 (Weight of BIT chips)

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: PSEUDO RANDOM PATTERN GENERATOR (PRPG) & MULTIPLE INPUT SHIFT REGISTER (MISR)

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

III) PENALTY EQUATIONS (CONT)

c) POWER (mW)

Maximum power of BIT chips = (1410)n1 + (1005)n2 + (165)n3

d) TIME

TEST TIME = v5 +(v3)(v4)

PARAGRAPH 6.10

COMPARATOR TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR	
CATEGORY: SHORT TUTORIAL	PAGE 1 of 4
SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE	

DATA TYPE: TEXT [x] LIST [ ] TABLE [ ] GRAPHIC [ ] EQUATIONS [ ]

DATA:

SHORT TUTORIAL
FOR
COMPARATOR

Comparators can readily be incorporated into your hardware designs to achieve Built-In-Test (BIT) capability for a large variety of functions with minimum expense. With this approach, Circuit Under Test (CUT) test stimuli, which is generated by the Line Replaceable Module (LRM), is applied to a CUT and the output of the CUT is applied to a comparator along with a reference signal. If the output of the CUT exceeds any predetermined difference with respect to the reference signal an output will be generated from the comparator which will be used as a TEST FAIL signal. For some applications, it will be necessary to process the CUT output with the addition of a signal processing circuit and then feed the result into a comparator.

The COMPARATOR BIT TECHNIQUE allows for either including a signal source as part of the bit hardware or for receiving the test signal from outside the LRM. If multiple channels are present on the CUT, multiplexers can be added to distribute the test signal to various channel inputs and to distribute the CUT outputs to the comparator for analysis.

Due to the wide variety of processing circuits available, (eg. frequency to voltage converters, sample and hold circuits), together with the benefits gained from signal multiplexing, the COMPARATOR BIT TECHNIQUE lends itself to a wide variety of applications.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR	
CATEGORY: SHORT TUTORIAL	**PAGE** 2 **of** 4
SUBCATEGORY: 1. LEVEL I BLOCK DIAGRAM 2. BIT SEQUENCE FLOW CHART	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2

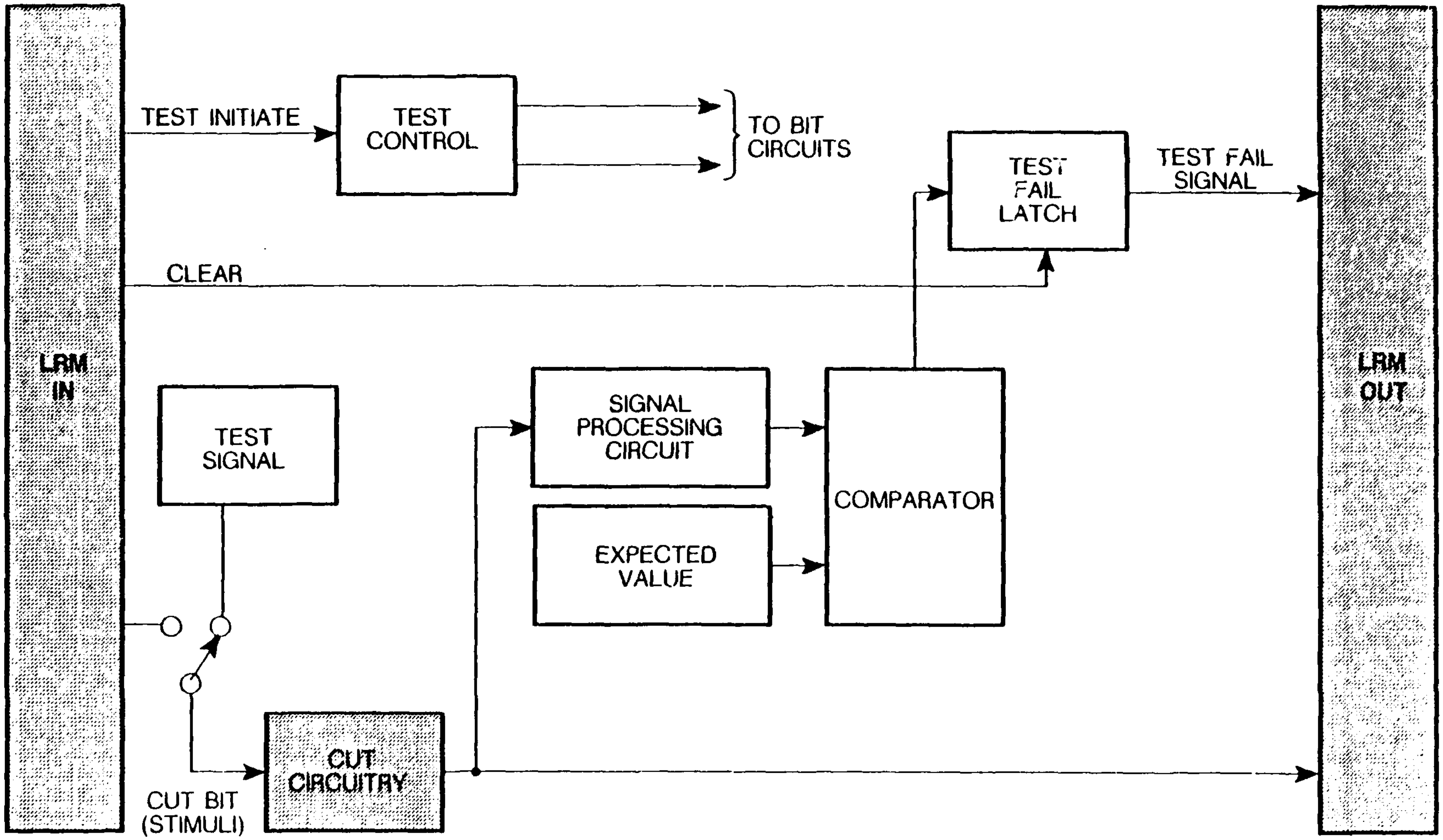
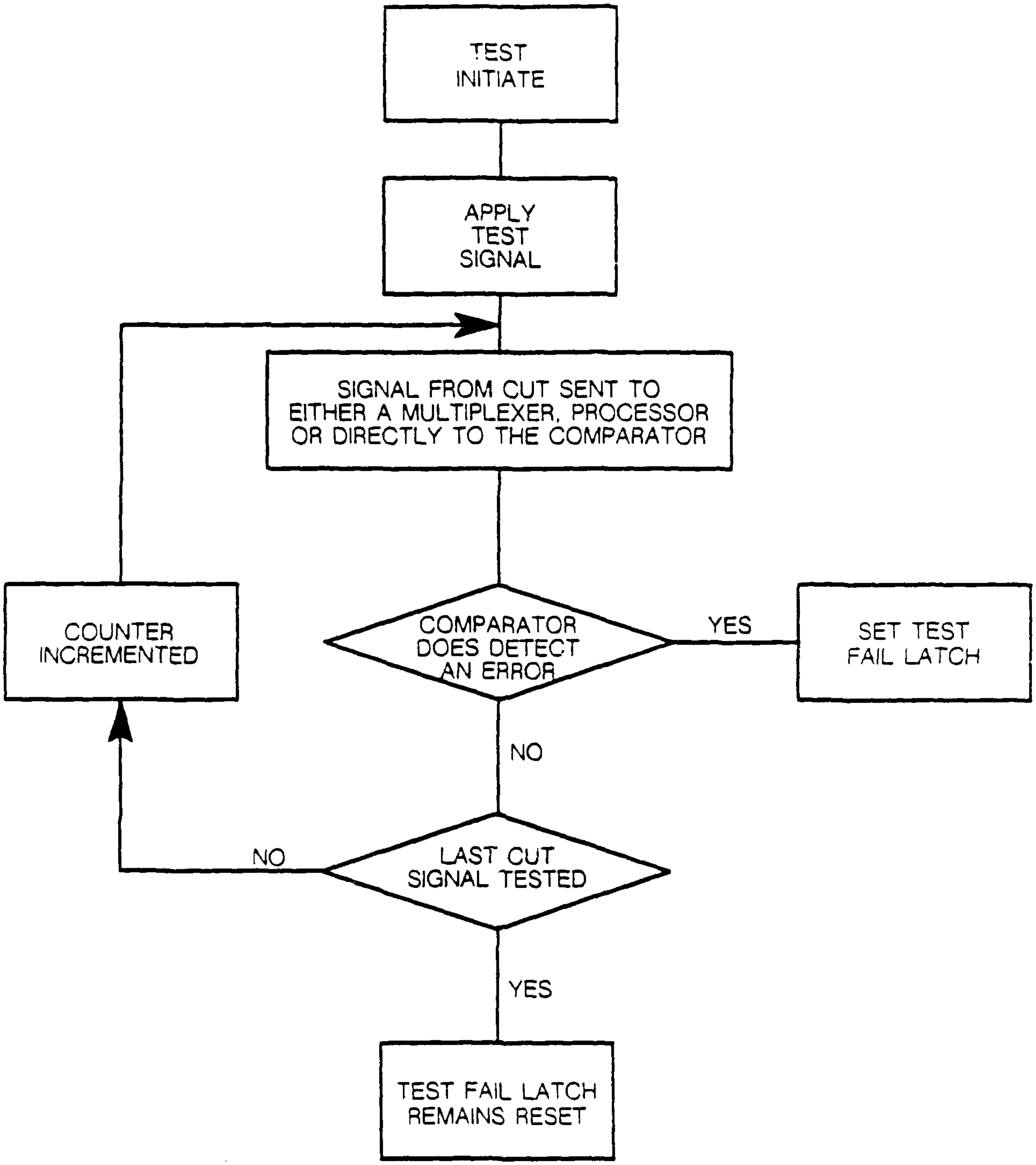


FIGURE 1 LEVEL I BLOCK DIAGRAM UTILIZING COMPARATORS AS A BIT TECHNIQUE



FIGUE 2 BIT SEQUENCE FLOW CHART FOR UTILIZING COMPARATOR TESTING TECHNIQUES FOR N CHANNELS OR SIGNALS

PAGE 4 of 4

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR	
CATEGORY: LONG TUTORIAL	PAGE 1 of 12
SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
COMPARATOR

1. A Test Initiate signal is received by the test control logic which disconnects the primary inputs to the CUT.

2. A Test Signal is applied to the inputs of the CUT.

3. An output signal from the CUT, is routed to either a multiplexer, signal processor or directly to the input of the Comparator circuit where it is compared against an expected value or function. If a difference between the expected value and the CUT input to the comparator is observed then the TEST FAIL latch is set and a TEST FAIL signal is generated. If the comparator does not detect a difference between the expected value and the CUT signal the TEST FAIL latch remains reset and the TEST FAIL signal remains deactivated.

4. If multiple signals are to be BIT tested, the counter is incremented and step 3 is repeated until all of the CUT signals are BIT tested.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

COMPARATOR
ADVANTAGES

The use of comparators as a Built In Test tool offers the following advantages to the circuit designer:

- The use of comparators can be applied to verify a large variety of functions such as:
  - Voltage levels
  - Sine Waves
  - Triangle Waves
  - Square Waves
  - Minimum Possible Input Value
  - Maximum Possible Input Value
  - Average Input Value
- Comparators can be purchased readily from many manufacturers on an off-the-shelf basis in a variety of package types thereby minimizing availability and packaging problems.
- Comparators can be purchased which are compatible with all forms of logic.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

COMPARATOR
ADVANTAGES
(CONT)

- The basic component of comparators is the Operational Amplifier (Op Amp) which possesses the following advantages:
  - The input impedance of Op Amps are extremely high thereby minimizing CUT loading problems when incorporated into a BIT circuit.
  - Op Amp bandwidths are very large (devices with bandwidths greater than 100 MHZ are available) thereby expanding signal testing capabilities.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE DISADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

COMPARATOR
DISADVANTAGES

The use of comparators as a Built In Test tool poses the following disadvantages to the circuit designer:

- The reference signal must be accurately maintained. Any deviation from the desired reference could cause erroneous BIT results.

- Frequently additional power supplies are required as either Op Amp power supplies or as reference voltage supplies.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

COMPARATOR
ATTRIBUTES

1. REAL ESTATE PENALTY

- The use of signal multiplexing with the comparator technique reduces the real estate penalty incurred in contrast to the use of concurrent techniques such as the redundancy technique. This is particularly true if large numbers of circuits are to be BIT tested.
- If signal processing circuits are required, the real estate penalty increases proportionately.
- Minimized due to the variety of package types available.
- Required real estate for implementation of the technique increases as the number of CUT signal tested increases. The possibility of minimizing the amount of real estate required can be achieved with the use of multiplexers.
- The addition of discrete components, needed for biasing, adds to the real estate penalty. For Window Comparator techniques, two discrete resistors must be added to create the high reference signal and two resistors must also be added to create the low reference signal. Resistors will also be required if hysteresis is desired in the comparator circuit. Zener diodes may also be needed for producing desired output levels.
- The addition of gating circuitry is frequently necessary for the purposes of enabling and latching.
- If Signal Processing circuits are required, besides the addition of Linear integrated circuits chips, peripheral supporting components such as resistors, and capacitors are frequently needed.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

COMPARATOR
ATTRIBUTES
(CONT)

2. POWER PENALTY

- The use of signal multiplexing in this technique, reduces the power penalty which develops with the use of other techniques such as the redundancy technique. This is particularly true if large numbers of circuits are to be BIT tested.

- If signal processing circuits are required, the power penalty increases proportionately.

3. RELIABILITY PENALTY

- As the quantity of comparators increases with the use of this technique reliability decreases proportionately.

4. TIMING PENALTY

- Throughput delays will occur because the CUT input and output signals must pass through the added BIT multiplexer.

5. CONCEPTUAL COMPLEXITY

- Straight forward.

6. TECHNOLOGY

- All current digital technology.

7. IS BITE SELF TESTABLE

- Yes with the addition of extra hardware.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

COMPARATOR
ATTRIBUTES
(CONT)

8. DESIGN COST

   - The use of the Comparator BIT Technique reduces design costs compared to concurrent techniques if large numbers of CUT circuits are to be BIT tested.
   - If signal processing circuits are required, the design costs increase proportionately.

9. WEIGHT PENALTY

   - The use of signal multiplexing reduces the weight penalty compared with concurrent techniques. This is particularly true if large numbers of circuits are to be BIT tested.
   - If signal processing circuits are required, the weight penalty increases proportionately.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐

DATA:

a) SEE FIGURE 3 FOR COMPARATOR BIT LEVEL II BLOCK DIAGRAM

b) SEE FIGURE 4 FOR COMPARATOR TEST SCHEMATIC DEFAULT DESIGN

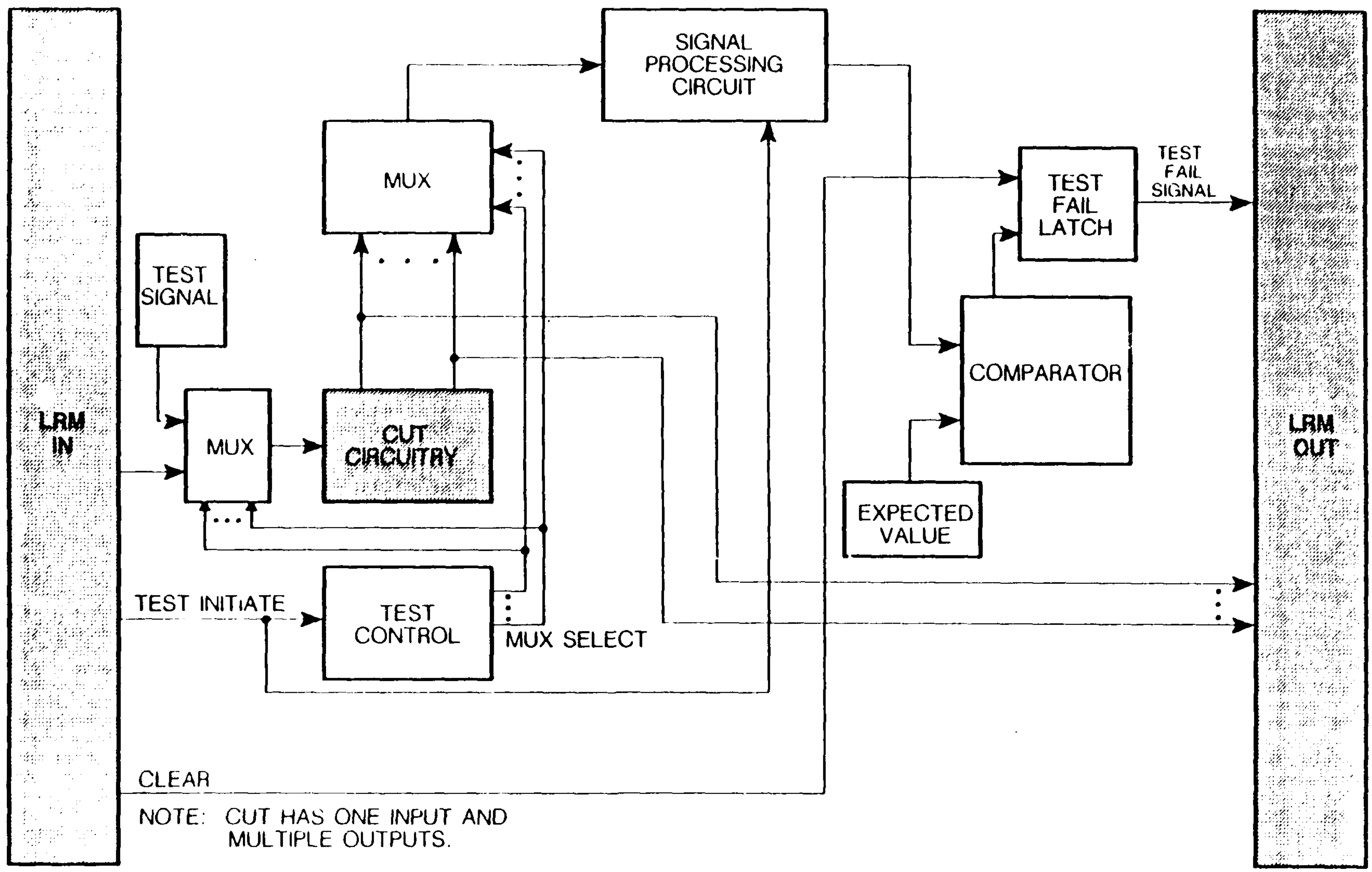
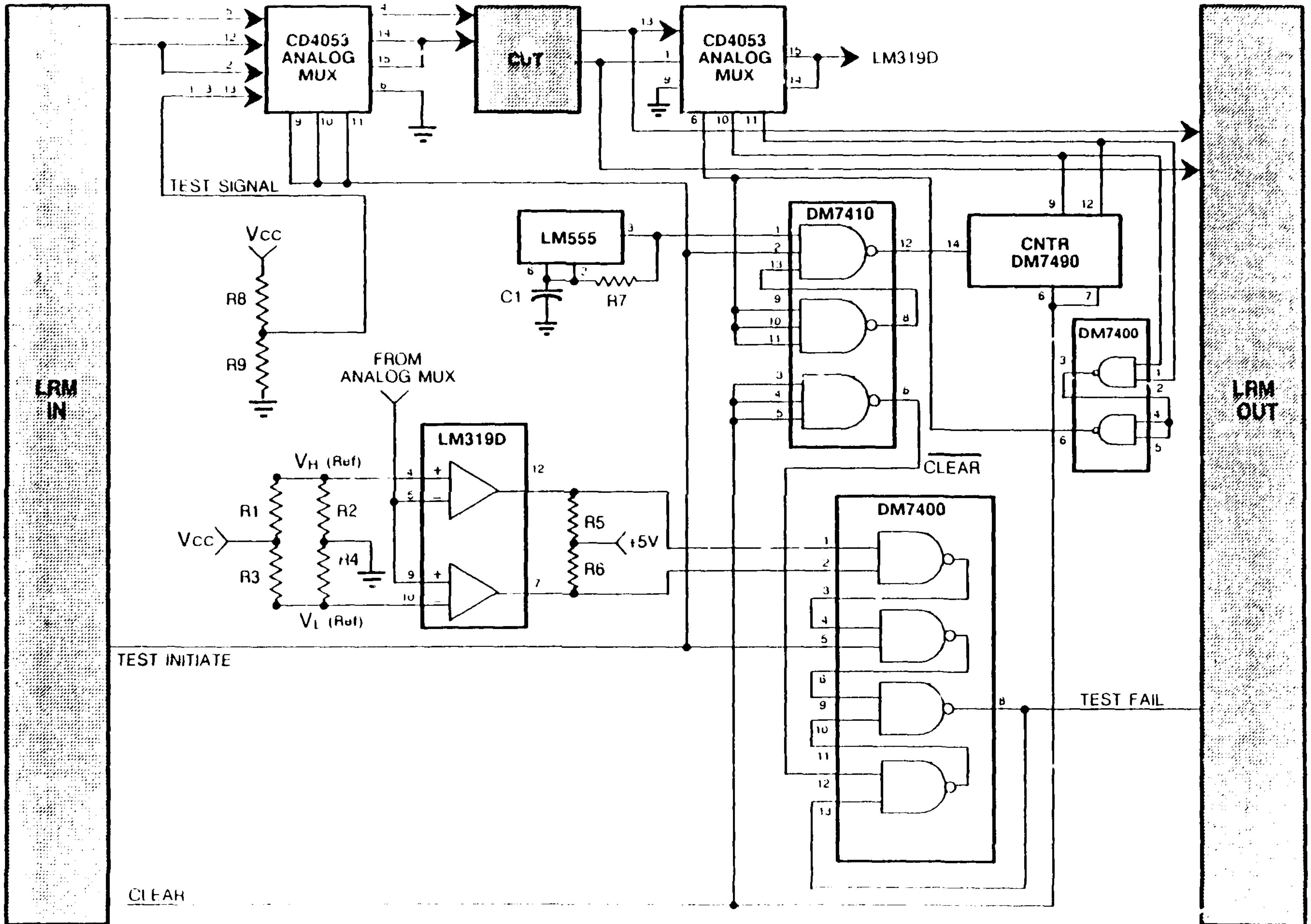


FIGURE 3 LEVEL II BLOCK DIAGRAM UTILIZING COMPARATORS AS A BIT TECHNIQUE



NOTE CUT HAS TWO INPUTS AND TWO OUTPUTS

FIGURE 4 COMPARATOR TEST SCHEME DEFAULT DESIGN

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR

CATEGORY: LONG TUTORIAL **PAGE** 11 **of** 12

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

NUMBER/NAME	AREA (sq in)	# OF PINS	POWER TYPICAL (mW)	POWER MAX. (mW)	WEIGHT (gms)
LM319D VOLTAGE COMPARATOR	0.2044	14	200	500	2
DM7400 QUAD DUAL INPUT NAND GATE	0.22	14	100	500	2
DM7410 TRIPLE THREE INPUT NAND GATE	0.22	14	100	500	2
LM555 TIMER	0.1	8	350	600	2
CD4053N ANALOG MULTIPLEXER	0.217	16	150	500	2
DM7490 COUNTER	0.22	14	145	500	2
CAPACITOR C1	0.681	2	50	250	3
RESISTORS R1 THRU R9	0.0225	2	100	250	2

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR	
CATEGORY: LONG TUTORIAL	PAGE 12 of 12
SUBCATEGORY: BIBLIOGRAPHY	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

NONE REQUIRED

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR	
CATEGORY: USER REQUESTED DATA	PAGE 1 of 1
SUBCATEGORY:	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

QUESTIONS	VARIABLE ASSIGNMENT
1. How many CUT signals to be tested?	v1
3. What is test time required for each signal?	v2

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR	
CATEGORY: EQUATIONS	**PAGE** 1 **of** 2
SUBCATEGORY: (NOT TO BE DISPLAYED)	

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITION

n1 = Number of LM319D Comparator chips required

n2 = Number of DM7400 Quad dual input nand gates required

n3 = Number of DM7410 Triple three input nand gates required

n4 = Number of resistors required

n5 = Number of capacitors required

n6 = Number of CD4053 Analog multiplexers required

n7 = Number of LM555 Timers required

n8 = Number of DM7490 Counters required

NOTE: Round off the values of n2 and n8 to the next highest whole number.

II) COMPONENT DETERMINATION EQUATION

n1 = 1

n2 = v1/4

n3 = 1

n4 = 9

n5 = 1

n6 = v1 + 1 For odd number of v1
= v1 For even number of v1

n7 = 1

n8 = v1/4

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: COMPARATOR

CATEGORY: EQUATIONS

SUBCATEGORY: (NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

III) PENALTY EQUATIONS

a) AREA (sq in)

Area of BIT chips = (0.2044)n1 + (0.22)n2 + (0.68)n3 + (0.225)n3 + (0.681)n5 + (0.217)n6 + (0.1)n7 + (0.068)n8

Total area of BIT circuitry = Area of BIT chips + 15% for PC traces = 1.15 (Area of BIT chips)

b) WEIGHT (gms)

Weight of BIT chips = (2)n1 + (2)n2 + (1)n3 + (2)n4 + (3)n5 + (2)n6 +(2)n[7] + (1)n[8]

Total weight of BIT circuitry = Weight of BIT chips + 10% for weight of solder = 1.1 (weight of BIT chips)

c) POWER (mW)

Total BIT circuitry power penalty for a specific number of CUT signals to be tested = (200)n1 + (100)n2 + (100)n3 + (100)n4 + (50)n5 + (150)n6 + (350)n7 + (145)n8

d) TEST TIME

Test Time = (v1)(v2)

PARAGRAPH 6.11

VOLTAGE SUMMING TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING	
CATEGORY: SHORT TUTORIAL	**PAGE** 1 **of** 4
SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE	
DATA TYPE: TEXT ☒ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

SHORT TUTORIAL
FOR
VOLTAGE SUMMING

Voltage summing is a concurrent analog Built-In-Test (BIT) technique whereby multiple voltage levels are added together using operational amplifiers. The resulting sum is then fed into a comparator circuit which compares the sum against a reference signal(s). The output of this comparator circuit generates a pass/fail signal. This technique is particularly useful for monitoring a set of power supply voltages.

This BIT technique is often used along with the comparator technique to test circuits with multiple output channels. Voltage summing BIT can also be used in conjunction with redundancy BIT techniques.

LIBRARY ELEMENT DATA SHEET

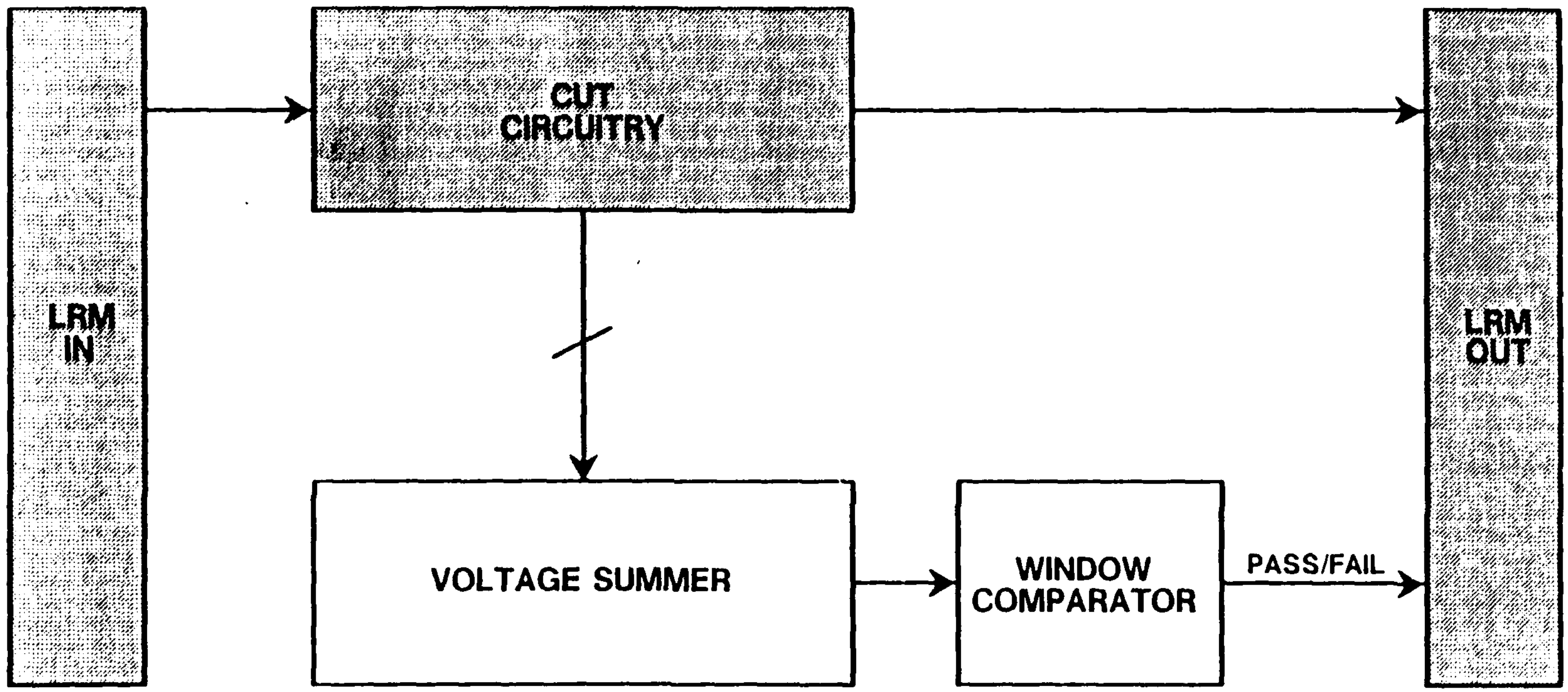
BIT TECHNIQUE: VOLTAGE SUMMING	
CATEGORY: SHORT TUTORIAL	PAGE 2 of 4
SUBCATEGORY: 1. LEVEL I BLOCK DIAGRAM 2. BIT SEQUENCE FLOW CHART	

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2



UNSHADED BOXES REPRESENT BIT CIRCUITRY.

FIGURE 1 LEVEL I BLOCK DIAGRAM
VOLTAGE SUMMING TECHNIQUE

PAGE 3 of 4

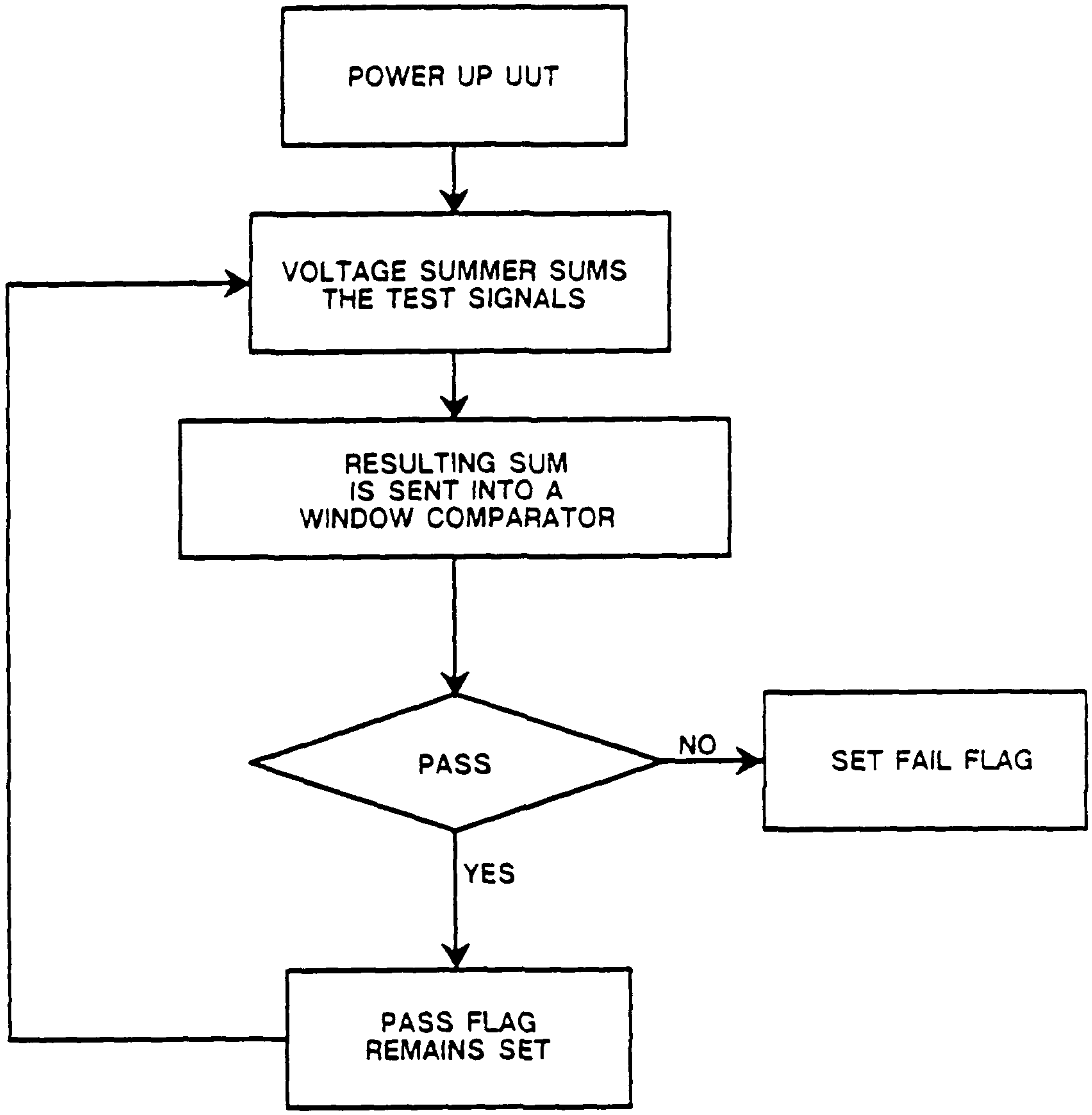


FIGURE 2 BIT TEST SEQUENCE FLOW CHART FOR VOLTAGE SUMMING BIT TECHNIQUE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING	
CATEGORY: LONG TUTORIAL	PAGE 1 of 10
SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
VOLTAGE SUMMING

1. Unit Under Test (UUT) is powered up.

2. The voltage levels to be monitored are routed into a voltage summing circuit. This circuit adds the separate voltage levels and outputs the resulting sum.

3. The sum is then sent into a window comparator circuit which checks the signal against an upper and lower reference voltage.

4. If the sum is within the upper and lower reference voltages, the PASS/FAIL output remains high indicating a PASS condition. If the sum is out of specification, the PASS/FAIL output signal goes low indicating a FAIL condition.

5. The sum is continuously monitored by the window comparator. The PASS/FAIL output signal remains high (PASS) unless a failure is encountered.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

VOLTAGE SUMMING ADVANTAGES

The Voltage Summing BIT technique provides the following advantages to the circuit designer:

- A minimum of components and Line Replaceable Module (LRM) real estate are required to implement a Voltage Summing BIT as compared with other BIT techniques such as Comparator BIT.

- The real estate savings increases proportionally to the number of voltage level outputs to be monitored.

- Voltage Summing BIT is a concurrent test, therefore end-to-end run time is not compromised. In addition, a failure will be detected anytime it occurs during normal operation.

The basic component of a voltage summing circuit is the op amp which possesses the following advantages:

- The input impedance of an op amp is extremely high, thereby minimizing Circuit Under Test (CUT) loading problems when incorporated into a BIT circuit.

- Operational Amplifiers (Op Amps) are readily available off the shelf from a large number of manufacturers.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING	
CATEGORY: LONG TUTORIAL	**PAGE** 3 **of** 10
SUBCATEGORY: BIT TECHNIQUE DISADVANTAGES	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

VOLTAGE SUMMING
DISADVANTAGES

The Voltage Summing BIT technique poses the following disadvantages to the circuit designer:

- The ability to verify the specification requirement of an individual voltage level is reduced because only the sum of the voltage levels is monitored.
- Reference voltages used in the window comparator must be provided and accurately maintained.
- Voltage Summing BIT can only be used to monitor static signals.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

VOLTAGE SUMMING
ATTRIBUTES

1. REAL ESTATE PENALTY

   - 1 op amp configured as a voltage summing amplifier.
   - 2 comparators configured as a window detector.
   - 1 flip flop used as a latch.
   - The number of resistors needed is directly proportional to the number voltage levels to be summed and may be calculated using the following equation:

     Number of resistors = number of voltage levels to be summed + 9

2. POWER PENALTY

   - Proportional to the number of voltage levels to be summed. This is due to the fact that each voltage is sent through an input resistor as part of the summing circuit. Additionally, the power dissipation of the op amp, flip flop, and two (2) comparators must be considered.

3. RELIABILITY PENALTY

   - Proportional to the Mean Time Between Failures (MTBF) of the op amp, 2 comparators, and one (1) flip flop used.
   - The MTBF of the resistors is so great that they need not be in the reliability equation.

4. TIMING PENALTY

   - Since Voltage Summing BIT is done concurrently, there is no timing penalty.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING	
CATEGORY: LONG TUTORIAL	**PAGE** 5 **of** 10
SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

VOLTAGE SUMMING
ATTRIBUTE
(CONT)

5. CONCEPTUAL COMPLEXITY

   - Circuit design is relatively simple.
   - Totally hardware in design.

6. TECHNOLOGY

   - Analog circuitry

7. IS BITE SELF TESTABLE?

   - Voltage summing can be made self testable with the addition of additional circuitry.

8. DESIGN COST

   - All components used are readily available at low cost.
   - Minimal engineer man-hours required to design and debug circuitry.

9. SOFTWARE DESIGN COST

   - None

10. WEIGHT

   - Nominal weight is equal to the weight of the 1 op amp, 2 comparators, flip flop, and 9 resistors.
   - Weight increases as the number of voltage levels to be summed increases due to the addition of input resistors.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING	
CATEGORY: LONG TUTORIAL	PAGE 6 of 10
SUBCATEGORY: DEFAULT DESIGN	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

a) SEE FIGURE 3 FOR VOLTAGE SUMMING TECHNIQUE LEVEL II BLOCK DIAGRAM

b) SEE FIGURE 4 FOR VOLTAGE SUMMING DEFAULT DESIGN

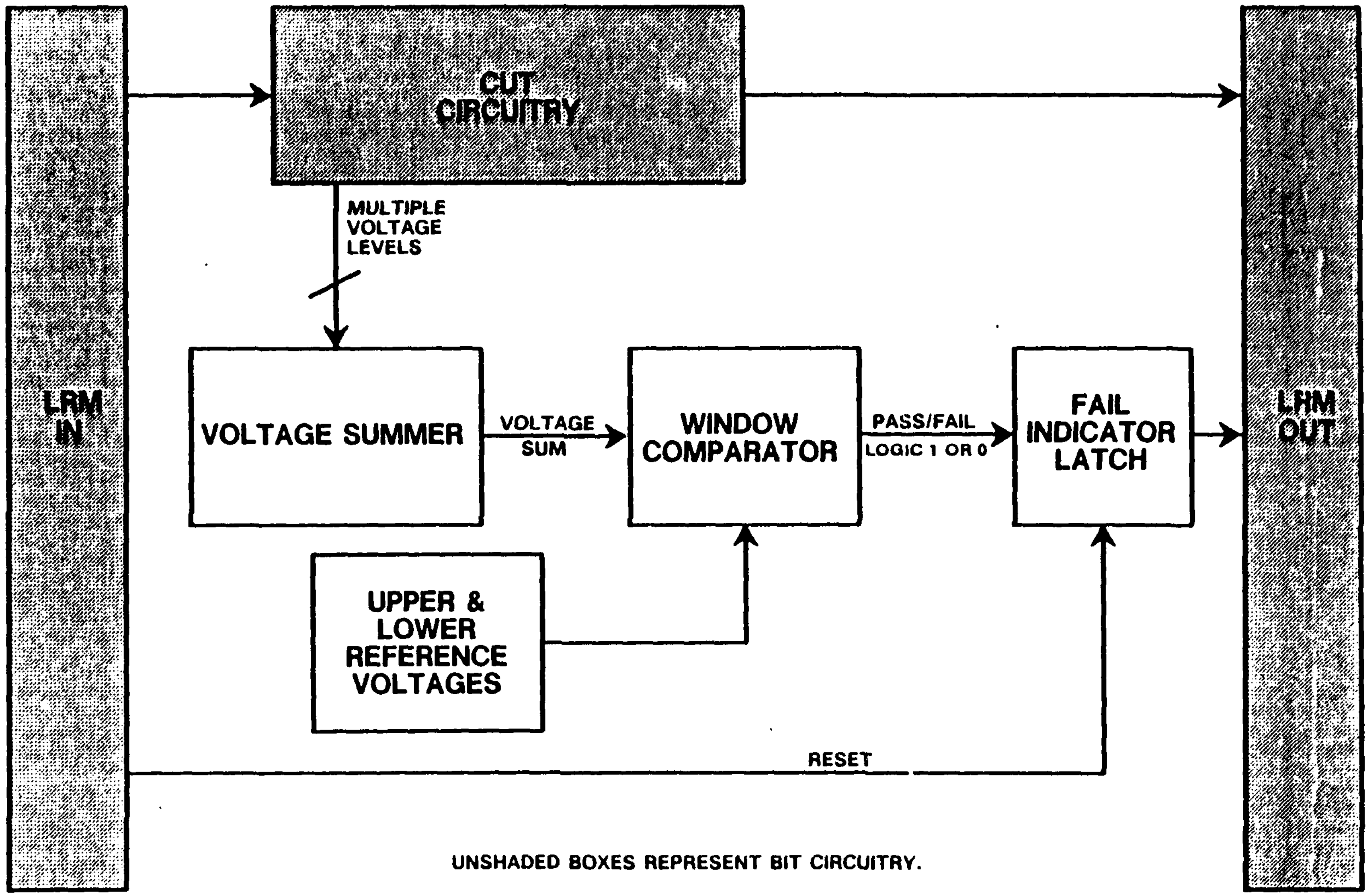


FIGURE 3 LEVEL II VOLTAGE SUMMING TECHNIQUE

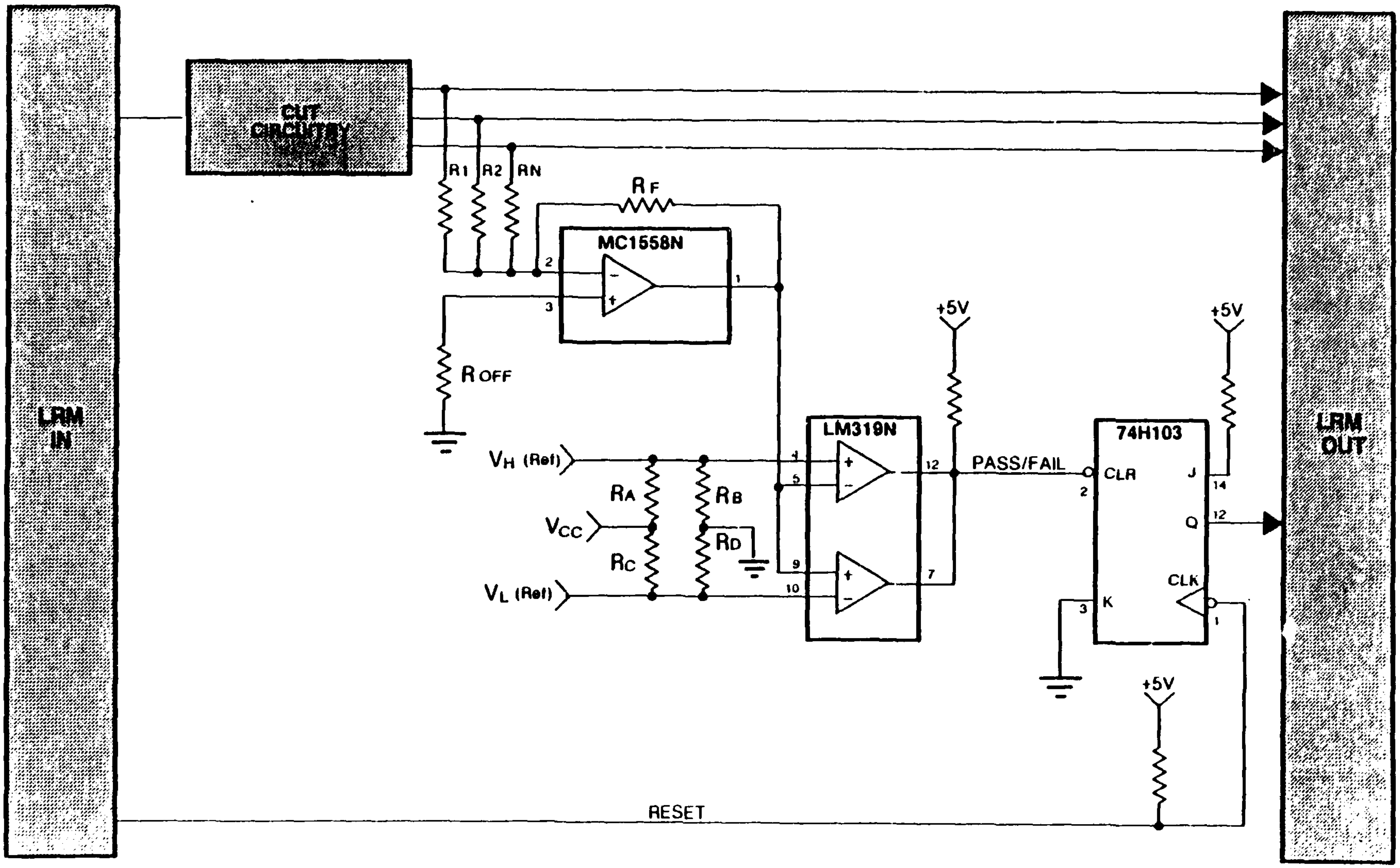


FIGURE 5 DEFAULT DESIGN - VOLTAGE SUMMING

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING

CATEGORY: LONG TUTORIAL

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

NUMBER/NAME	AREA *(sq in)*	# OF PINS	POWER TYPICAL *(mW)*	POWER MAX. *(mW)*	WEIGHT *(gms)*
LM319N/ COMPARATOR	0.19	14	300	500	2.0
MC1558/ OP AMP	.09	8	300	500	1.3
74H103/ JK FLIP FLOP	.20	14	250	550	0.9
R1 - Rn	.03	—	—	250	0.2
Ra - Rd	.03	—	—	250	0.2
Rf	.03	—	—	250	0.2
Roff	.03	—	—	250	0.2
R (pullups)	.03	—	—	250	0.2

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING	
CATEGORY: LONG TUTORIAL	**PAGE** 10 **of** 10
SUBCATEGORY: BIBLIOGRAPHY	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

NONE REQUIRED

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING

CATEGORY: USER REQUESTED DATA

SUBCATEGORY:

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

QUESTIONS	VARIABLE ASSIGNMENT
1. How many voltages are to be summed?	v1
2. What are the values of Vcc?	v2
3. What are the values of Ra?	v3
4. What are the values of Rb?	v4
5. What are the values of Rc?	v5
6. What are the values of Rd?	v6
7. What are the values of Roff?	v7
8. What is the sum of the input voltage to be monitored?	v8

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITION

BIT CHIPS USED:

n1 = Number of comparator chips

n2 = Number of flip-flop chips

n3 = Number of op amp chips

DISCRETE COMPONENTS USED:

n4 = Number of input resistors

n5 = Number of feedback resistors

n6 = Number of voltage divider resistors

n7 = Number of bias current resistor

n8 = Number of pullup resistors

v1 = Number of voltages to be summed

v2 = Value of Vcc

v3 = Value of Ra

v4 = Value of Rb

v5 = Value of Rc

v6 = Value of Rd

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITION (CONT)

v7 = Value of Roff

v8 = Value of Vintot

II) COMPONENT DETERMINATION EQUATIONS

n4 = v1

III) PENALTY EQUATIONS

a) AREA (sq in)

AREA of BIT chips = (.19)n1 + (.20)n2 + (.09)n3 = .48

Area of BIT discrete components =
(.03)n4 + (.03)n5 + (.03)n6 + (.03)n7 +
(.03)n8 = .27 + (.03)n4

Total area of BIT circuitry = (Area of BIT chips) +
(Area of discrete components) + 15% For PC traces = .48 + .27 + (.03)n4 +
.15(.48 + .27 + (.03)n4) = .75 + (.03)n4 + .1 + .15(.03)n4
= .76 + (.034)n4

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: VOLTAGE SUMMING

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

II) PENALTY EQUATIONS (CONT)

b) WEIGHT (gms)

Total weight of BIT chips = (2.0)n1 + (.9)n2 + (1.3)n3 = 4.2

Total weight of BIT discrete components = (.2)n4+ (.2)n5 + (.2)n6 + (.2)n7 + (.2)n8 = 1.6 + (.2)n4

Total weight of BIT circuitry = (Weight of BIT chips) + (Weight of discrete components) + (Weight of solder) = (4.2 + 1.6 + .2n4) + .1(4.2 + 1.6 + .2n4)
= (5.8 + .2n[4])1.1

c) POWER (mW)

Total power consumption of BIT chip = (300)n1 + (250)n2 + (300)n3 = 850

Discrete components' power consumption = (v2)(v2)[1/v3 + v4) + 1/(v5 + v6) + (v8)(v8)/v7]

Total power consumption = power consumption of BIT chips + power consumption of discrete components

d) TEST TIME

Since voltage summing BIT is executed concurrently, there is no test time penalty.

PARAGRAPH 6.12

REDUNDANCY TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY	
CATEGORY: SHORT TUTORIAL	**PAGE** 1 **of** 4
SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE	
DATA TYPE: TEXT [x] LIST [ ] TABLE [ ] GRAPHIC [ ] EQUATIONS [ ]	

DATA:

SHORT TUTORIAL
FOR
UTILIZING REDUNDANCY

Redundant test techniques can be implemented on a concurrent basis by the design engineer as a Built-In-Test (BIT) Tool. The approach taken is to include a standard (also known as a golden device) onto the Line replaceable Module (LRM). The Standard is an electrical replica of the Circuit Under Test (CUT) which requires BIT capability. The outputs from the CUT and the Standard are fed into a differential amplifier circuit which in turn feeds its output into a window comparator. The window comparator is designed to generate a Test Fail signal if the differential output signal is either greater than a positive reference level or more negative than a negative reference level.

A second standard can also be added to provide three identical circuits. The outputs of the three circuits can then be fed into a voting circuit. This scheme will provide a fault tolerant operation in addition to fault detection.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY	
CATEGORY: SHORT TUTORIAL	**PAGE** 2 **of** 4
SUBCATEGORY: 1. LEVEL I BLOCK DIAGRAM 2. BIT SEQUENCE FLOW CHART	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2

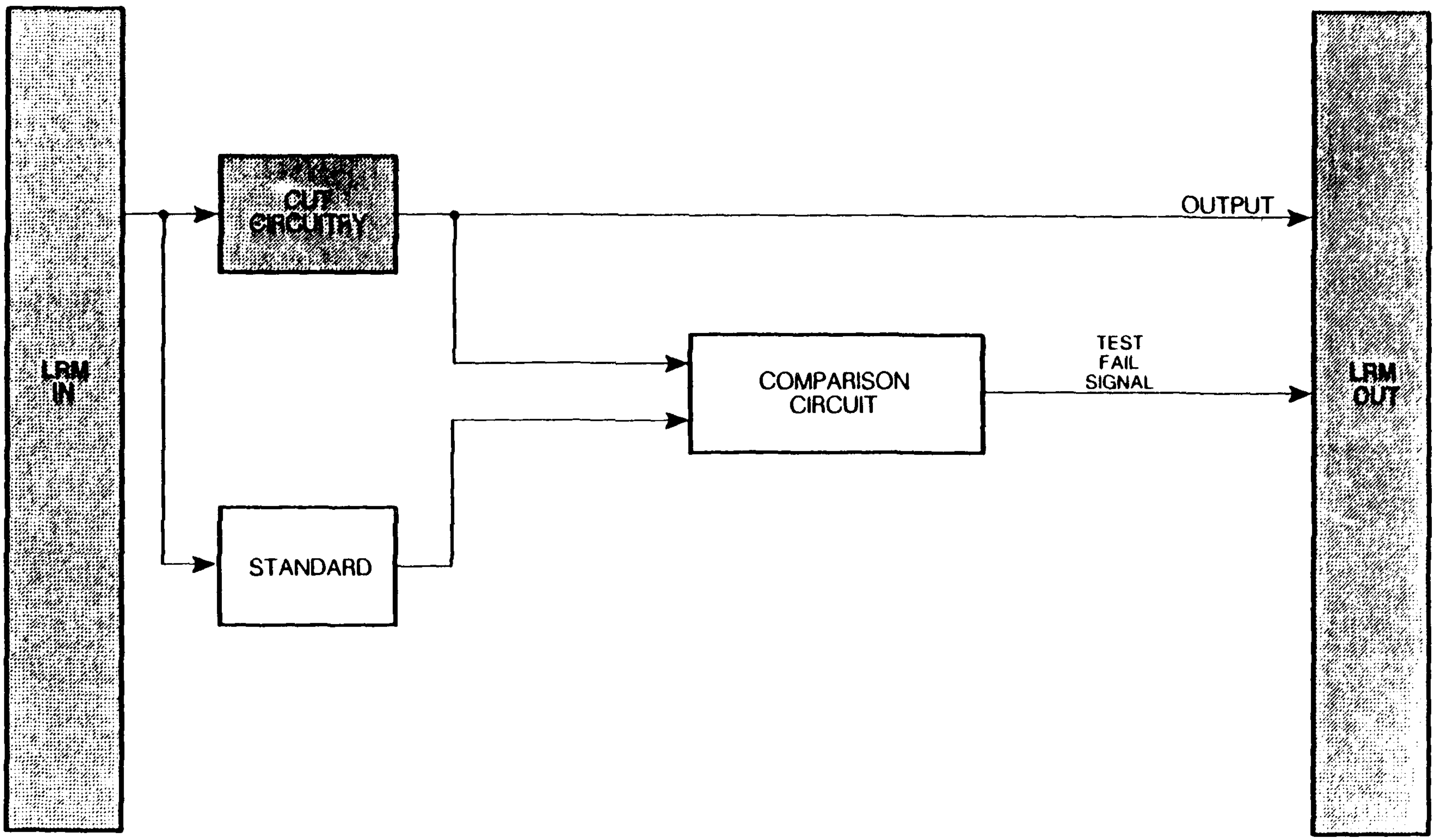


FIGURE 1 LEVEL I BLOCK DIAGRAM UTILIZING REDUNDANCY

PAGE 3 of 4

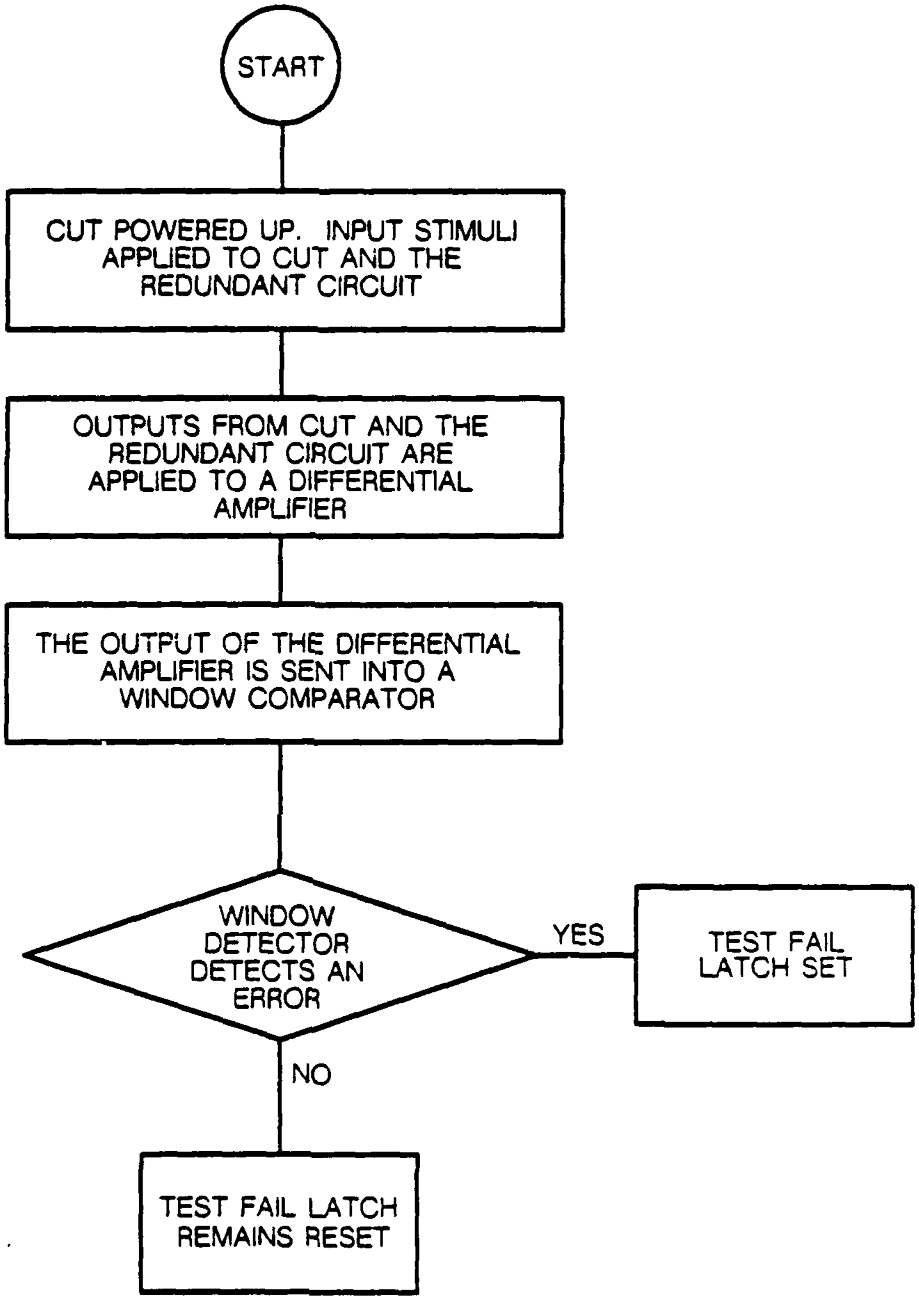


FIGURE 2 BIT SEQUENCE FLOW CHART FOR REDUNDANCY BIT TECHNIQUE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
UTILIZING REDUNDANCY

1. Signals sent to the CUT are sent concurrently to a replica of the CUT (a standard) during operation of the LRM.

2. Both the CUT output and the output from the standard are sent to a differential amplifier which provides an output which is proportional to the difference between the two signals.

3. The output of the differential amplifier is sent to the inputs of a window detector where they are compared to positive and negative reference voltages.

4. A Test Fail signal is generated if either the CUT output is more positive or more negative than the reference voltages.

5. The Test Fail latch is set with the detection of an error by the Window Detector, otherwise the Test Fail Latch remains reset.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY	
CATEGORY: LONG TUTORIAL	**PAGE** 2 **of** 10
SUBCATEGORY: BIT TECHNIQUE ADVANTAGES	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

UTILIZING REDUNDANCY
ADVANTAGES

Using Redundancy offers the following advantages to the circuit designer:

1. The technique is run on a concurrent basis therefore no time is lost to test the CUT.

2. All the circuit design must have been previously done for the CUT, therefore it is also readily available for the standard.

3. The technique offers the potential for increasing the reliability of the LRM with the addition of a second standard. The three outputs can then be fed into a voting circuit to provide fault tolerance.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE DISADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

UTILIZING REDUNDANCY
DISADVANTAGES

The use of the Redundancy technique possesses the following disadvantages:

1. In high frequency or critical timing applications, it may be difficult to synchronize the CUT output signals to the output of the redundant circuit.

2. Large amounts of real estate will be consumed because the technique doubles the circuit area required.

3. For a large number of CUT outputs, many differential amplifier and comparator BIT circuits would be required.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY	
CATEGORY: LONG TUTORIAL	**PAGE** 4 **of** 10
SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

UTILIZING REDUNDANCY
ATTRIBUTES

1. REAL ESTATE CONSIDERATIONS:

   * The amount of real estate required for this technique is equivalent to the size of the CUT plus the amount of real estate required for the differential amplifier, the window comparator and the Test Fail latch.

2. POWER CONSIDERATIONS:

   * The increase in power dissipation with the use of this technique is equivalent to the amount of power dissipated by the CUT plus the power dissipated by the differential amplifier, the comparator circuit and the Test Fail latch.

3. RELIABILITY CONSIDERATIONS:

   * With the use of this technique, failure rates increase proportionately to the circuit density and complexity of the CUT. The failure rates for the differential amplifier, comparator circuit and Test Fail latch must also be added to the total LRM failure rate.

4. TIMING CONSIDERATIONS:

   * No timing penalty is incurred with the use of this technique since it is run in the concurrent mode.

   * If high frequency or critical timing specifications are required by the CUT then difficulties may arise when attempting to synchronize the CUT's output with the output of the standard.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

UTILIZING REDUNDANCY
ATTRIBUTE
(CONT)

5. CONCEPTUAL COMPLEXITY

   * Straight forward

6. TECHNOLOGY

   * All current digital technologies

7. IS BITE SELF TESTABLE?

   * Since the cut is duplicated by the bit circuitry, a failure in either the cut or bit circuitry is detectable, therefore, the majority of the circuitry added for bit is checked out. Only the differential amplifier and window comparator circuits are not verified operationally.

8. DESIGN COST:

   * The cost of implementing Redundancy into a Computer Aided Design/Built-In-Test CAD/BIT design is proportional to the cost of the CUT circuit which is replicated, plus the cost of the differential amplifier and comparator.

9. WEIGHT CONSIDERATIONS:

   * The increase in weight is proportional to the weight of the CUT which is replicated plus the weight of the comparator circuit and the test fail latch.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY	
CATEGORY: LONG TUTORIAL	**PAGE** 6 **of** 10
SUBCATEGORY: DEFAULT DESIGN	
DATA TYPE: **TEXT** ☐ **LIST** ☐ **TABLE** ☐ **GRAPHIC** ☒ **EQUATIONS** ☐	

DATA:

a) SEE FIGURE 3 FOR UTILIZING REDUNDANCY LEVEL II BLOCK DIAGRAM

b) SEE FIGURE 4 FOR UTILIZING REDUNDANCY AS DEFAULT DESIGN

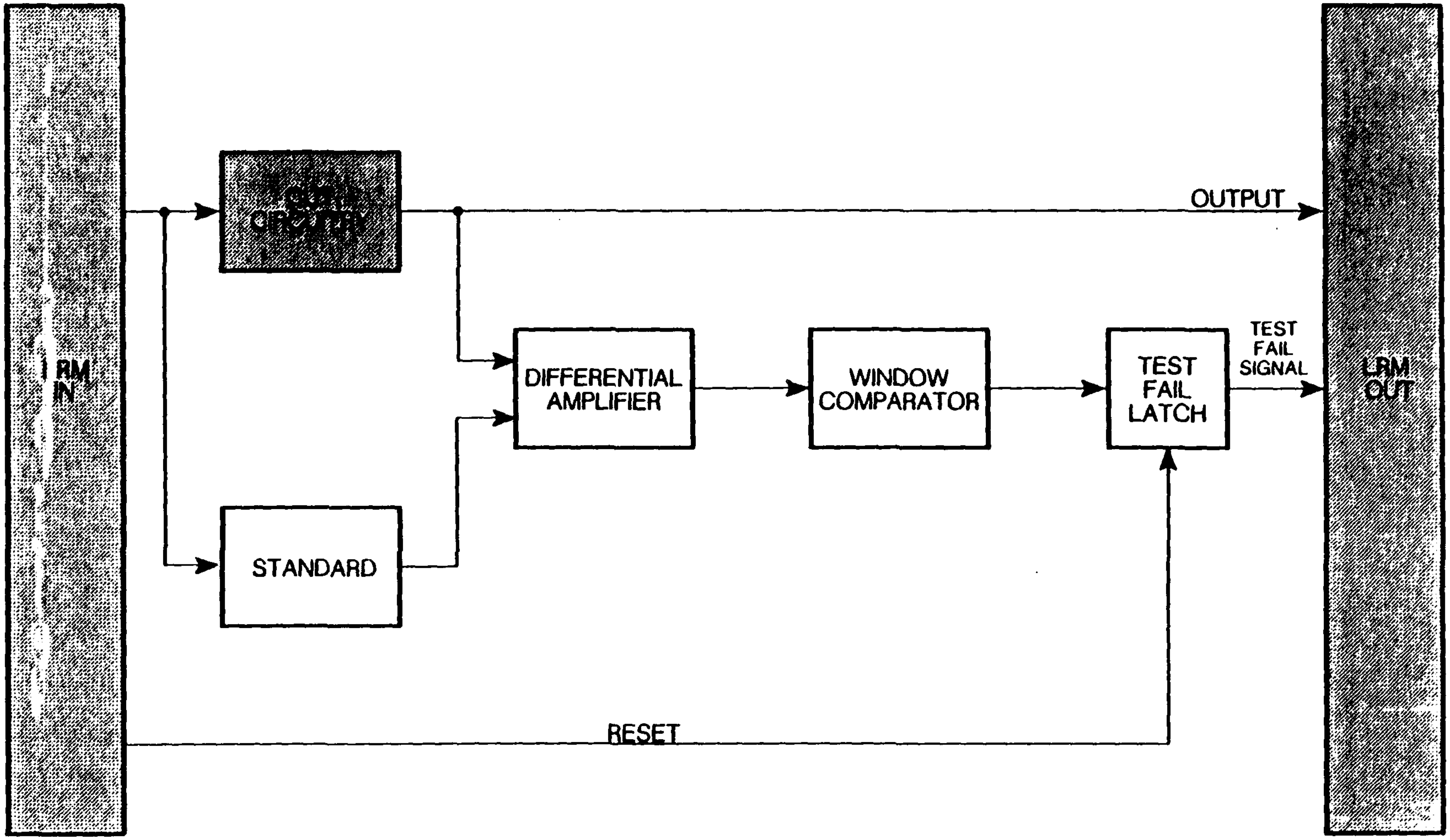


FIGURE 3 LEVEL II BLOCK DIAGRAM UTILIZING REDUNDANCY

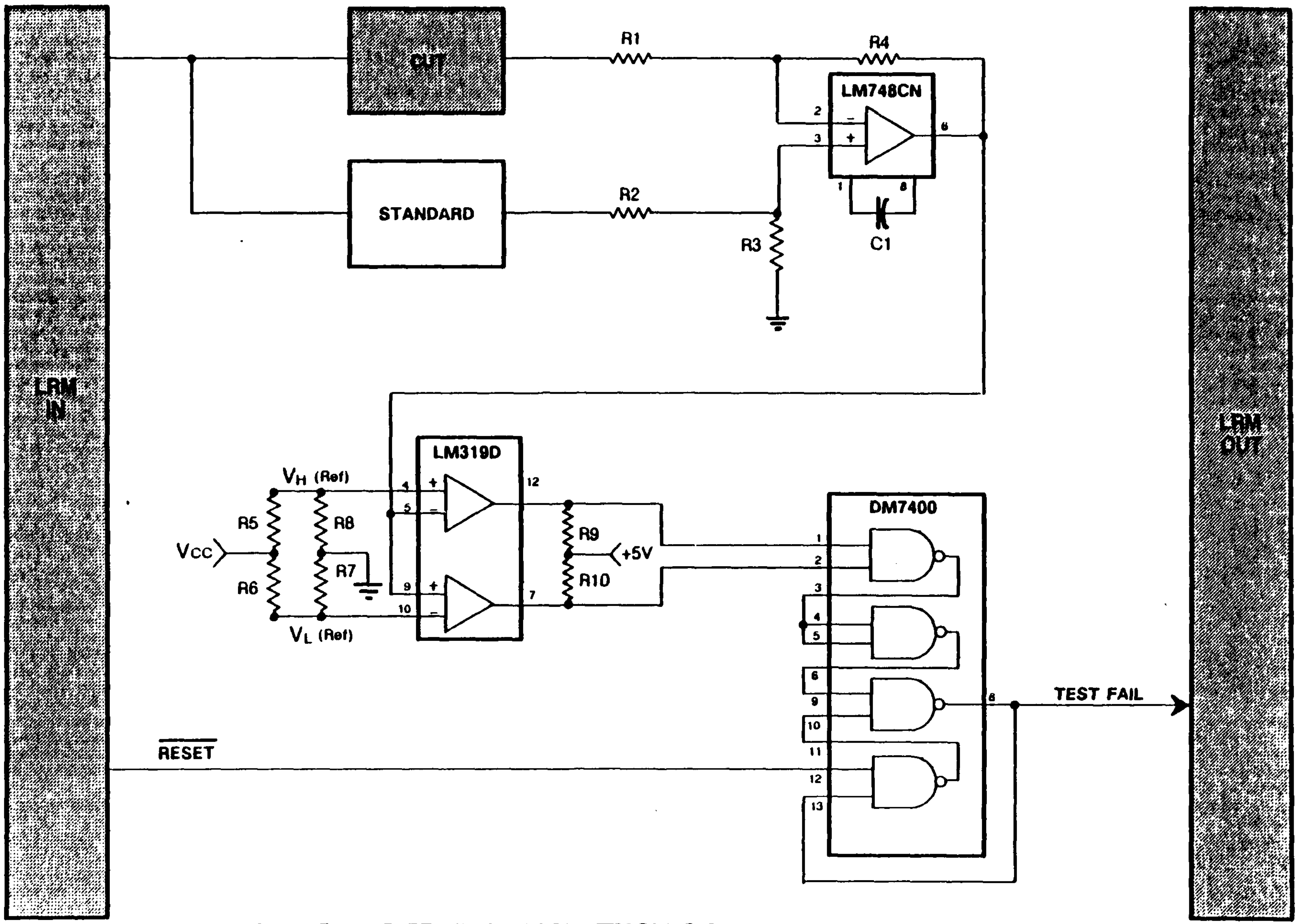


FIGURE 4 REDUNDANCY TEST SCHEME DEFAULT DESIGN

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY

CATEGORY: LONG TUTORIAL

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

NUMBER/NAME	AREA *(sq in)*	# OF PINS	POWER TYPICAL *(mW)*	POWER MAX. *(mW)*	WEIGHT *(gms)*
LM319D VOLTAGE COMPARATOR	0.2044	14	200	500	2
LM748CN OPERATIONAL AMPLIFIER	0.100	8	200	500	1
DM7400 QUAD DUAL INPUT NAND GATE	0.22	14	100	500	2
RESISTORS R1 THRU R10	0.0225	2	100	250	2
CAPACITOR C1	0.681	2	50	250	3

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY	
CATEGORY: LONG TUTORIAL	**PAGE** 10 **of** 10
SUBCATEGORY: BIBLIOGRAPHY	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

NONE REQUIRED

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY	
CATEGORY: USER REQUESTED DATA	**PAGE** 1 **of** 1
SUBCATEGORY:	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

QUESTIONS	VARIABLE ASSIGNMENTS
1. How many outputs are to be bit tested ?	v1

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITION

n1 = Number Of LM319 Comparator chips required

n2 = Number Of LM748 Operational Amplifiers

n3 = Number Of DM7400 Quad Dual Input Nand Gate chips required

n4 = Number Resistors required

n5 = Number Of capacitors required

v1 = Number of outputs to be tested

II) COMPONENT DETYERMINATION EQUATIONS

$n1 = v1$

$n2 = v1$

$n3 = v1$

$n4 = (10)v1$

$n5 = v1$

III) PENALTY EQUATIONS

a) AREA (sq in)

$$\text{Area of BIT chips} = (0.2044)n1 + (0.1)n2 + (0.22)n3 + (0.0225)n4 + (0.681)n5$$

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: UTILIZING REDUNDANCY

CATEGORY: EQUATIONS

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

III) PENALTY EQUATIONS (CONT)

b) WEIGHT (gms)

Weight of BIT circuitry = 2n1 + 910n2 + 2n3 + 2n4 + 3n5

Total weight of BIT circuitry = Weight of BIT chips + 10% for Weight of solder + Weight of CUT circuitry = 1.1 (Weight of BIT chips + Weight of CUT circuitry)

c) POWER (mW)

Total power penalty for the redundancy technique = n1(200) + n2(200) + n3(100) + n4(100) + n5(50)

NOTE: The power penalty is derived from typical power dissipation levels.

d) TEST TIMING

There is no timing penalty when using the redundancy BIT technique since the technique is run in the concurrent mode.

PARAGRAPH 6.13

ANALOG WRAPAROUND TECHNIQUE DATA PACKAGE

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND

CATEGORY: SHORT TUTORIAL

SUBCATEGORY: DESCRIPTION OF BIT TECHNIQUE

DATA TYPE: **TEXT** ☒ **LIST** ☐ **TABLE** ☐ **GRAPHIC** ☐ **EQUATIONS** ☐

DATA:

SHORT TUTORIAL
FOR
ANALOG WRAPAROUND

Analog wraparound is a non-concurrent Built-In-Test (BIT) technique. This consists of hardware and software (firmware in Read Only Memory (ROM)) and specifically requires a microprocessor, some Digital-to Analog (D/A) converters as output devices and some Analog-to-Digital (A/D) converters as input devices on board as part of the Circuit Under Test (CUT).

The technique consists of adding necessary circuitry so that upon a BIT INITIATE, the analog signal leaving the D/A output devices can be routed to the A/D input devices on the Line Replaceable Module (LRM). An appropriate BIT routine is stored in ROM along with test data to control the data transfer and compare the data received with the data transmitted. A mismatch will indicate a failure.

An option which the engineer may use to route the signal back to the microprocessor is to add an analog switch to wrap the signal leaving the D/A through the switch then to an A/D and back to a microprocessor.

Other forms of tests which can be performed are:

1. Amplifier/Attenuator stages
2. Transceiver/Receivers
3. Optical Links
4. Transducer coupling

Any function - complement pair can be tested using the wraparound method.

The Microprocessor BIT technique (a relative BIT technique), checks out the internal components of the microprocessor system. The wraparound BIT can be used to extend the microprocessor BIT to include the I/O.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND	
CATEGORY: SHORT TUTORIAL	**PAGE** 2 **of** 4
SUBCATEGORY: 1. LEVEL I BLOCK DIAGRAM 2. BIT SEQUENCE FLOW CHART	
DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐	

DATA:

SUBCATEGORY 1: SEE FIGURE 1

SUBCATEGORY 2: SEE FIGURE 2

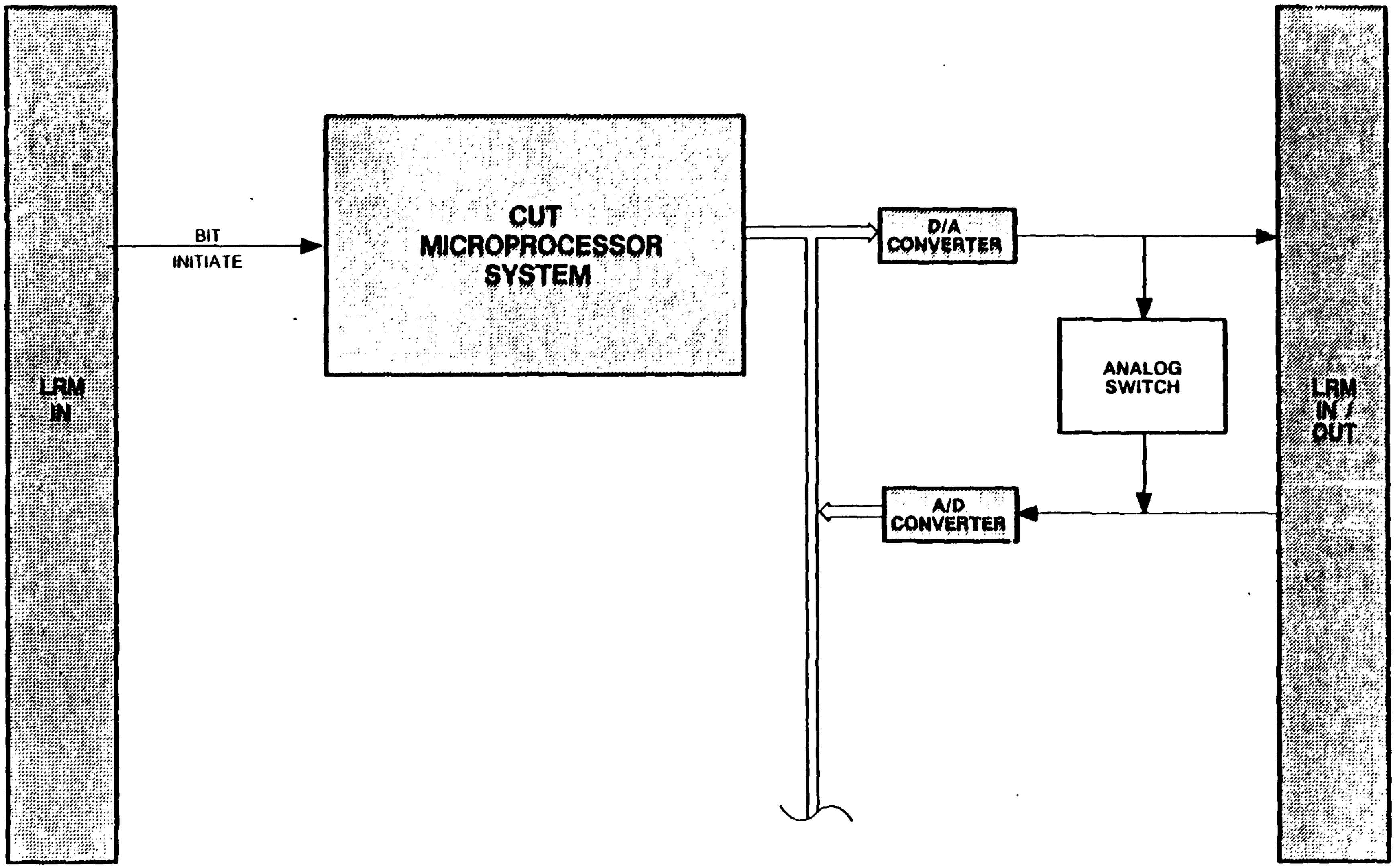


FIGURE 1 LEVEL I BOLCK DIAGRAM UTILIZING ANALOG WRAPAROUND

PAGE 3 of 4

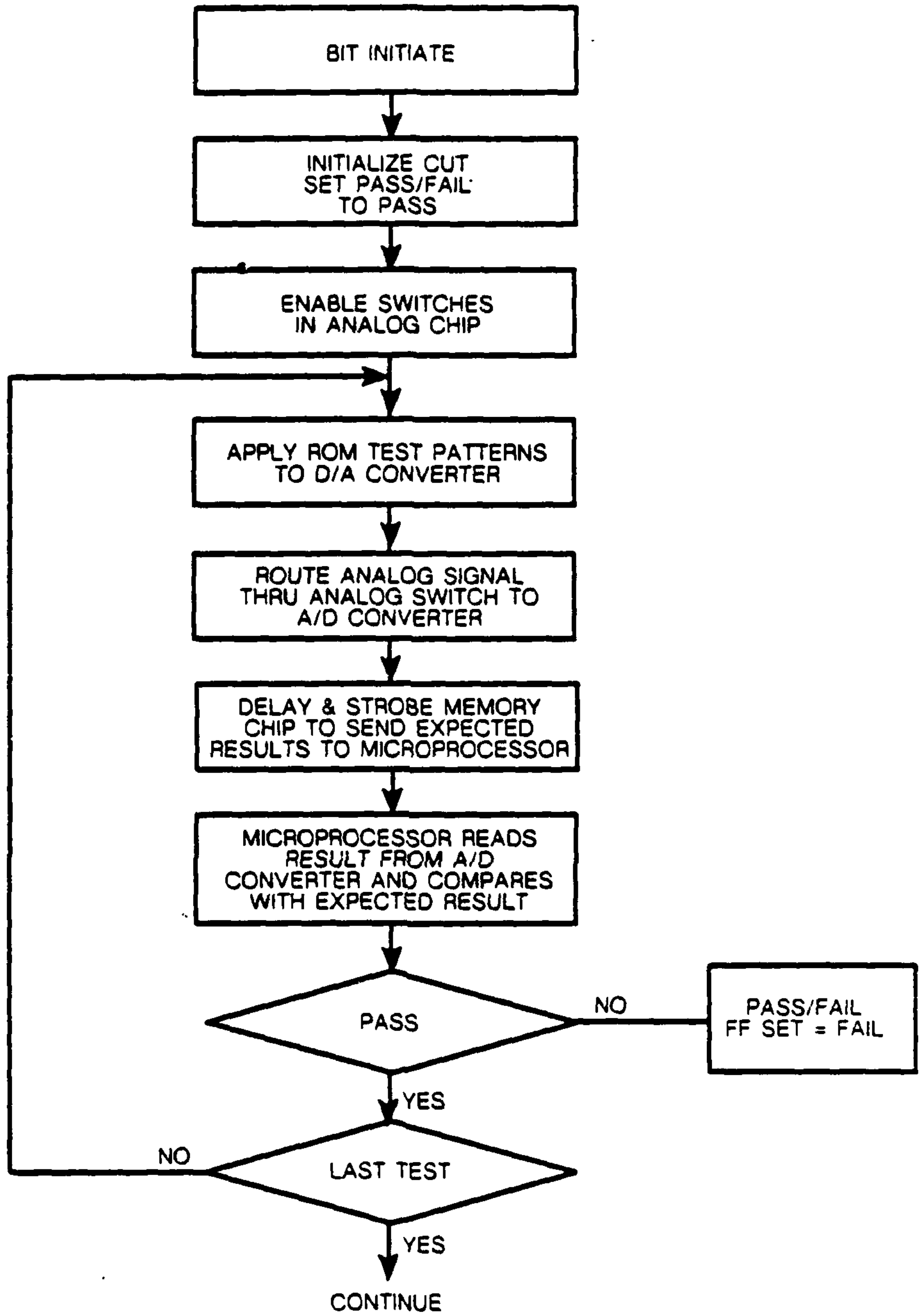


FIGURE 2 BIT SEQUENCE FLOW CHART
FOR ANALOG WRAPAROUND

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT SEQUENCE FLOW CHART DESCRIPTION

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

BIT SEQUENCE FLOW CHART DESCRIPTION
ANALOG WRAPAROUND

1. A 'BIT INITIATE' signal is input to the LRM, so testing can begin.
2. Initialize the Circuit Under Test and set the Pass/Fail equal to Pass.
3. Before applying a signal, enable the wraparound switches that are going to be used for that particular test.
4. Apply the ROM test patterns to the D/A converter(s).
5. At this point, the data is routed from the D/A converter through the proper enabled wraparound switches and into the A/D converter(s).
6. Delay and strobe the memory chip to send the expected results to the micro-processor.
7. Microprocessor reads the results from the A/D converter(s) and compares it with the expected result from memory.
8. If comparison fails, set Pass/Fail Flip-Flop to FAIL and end test. If comparison passes, continue.
9. If not the last ROM address, go back to STEP 4 and continue.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ADVANTAGES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ANALOG WRAPAROUND
ADVANTAGES

1. Only requires minimal hardware and is a conceptually simple design which is easy to implement.

2. Chips that are needed are readily available.

3. This technique may also be used in conjunction with "MICROPROCESSOR BIT", another Computer Aided Design/Built-In-Test (**CADBIT**) technique, to extend the BIT coverage to include the Input/Output (I/O) chips (which are not normally checked out with the Microprocessor BIT).

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND	
CATEGORY: LONG TUTORIAL	**PAGE** 3 **of** 10
SUBCATEGORY: BIT TECHNIQUE DISADVANTAGES	

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ANALOG WRAPAROUND
DISADVANTAGES

1. This technique only checks out a small portion of the LRM.

2. As the microprocessor system increases in size along with more D/A or A/D converters then the number of Analog chips must also increase (in quantity), therefore, increasing real estate and firmware requirements. Additional ROMs may be required to store the additional test patterns.

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND

CATEGORY: LONG TUTORIAL

SUBCATEGORY: BIT TECHNIQUE ATTRIBUTES

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

ANALOG WRAPAROUND
ATTRIBUTES

1. REAL ESTATE PENALTY
   - Minimal since most microprocessor LRMs have at most only a small number of D/A or A/D peripheral devices and analog switch packages are available with multiple switches in a package.
2. POWER PENALTY
   - Small - just requires additional power to wrap around switches.
3. RELIABILITY PENALTY
   - Small - the technique generally only requires a few analog switch chips which are not exceptionally unreliable.
4. TIMING PENALTY
   - generally small because number of test patterns required to test the D/As and A/Ds will not be extensive.
5. NON-CONCURRENT
6. CONCEPTUAL COMPLEXITY
   - Straight forward.
7. HARDWARE/SOFTWARE COMBO
   - Hardware
8. TECHNOLOGY
   - Digital & Analog chips resident.
9. Is BITE Self - Testable?
   - No

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND	
CATEGORY: LONG TUTORIAL	**PAGE** 5 **of** 10
SUBCATEGORY: DEFAULT DESIGN	

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☒ EQUATIONS ☐

DATA:

a) SEE FIGURE 3 FOR ANALOG WRAPAROUND LEVEL II BLOCK DIAGRAM

b) SEE FIGURE 4 FOR ANALOG WRAPAROUND DEFAULT DESIGN

c) SEE FIGURE 5 FOR ANALOG WRAPAROUND DEFAULT DESIGN

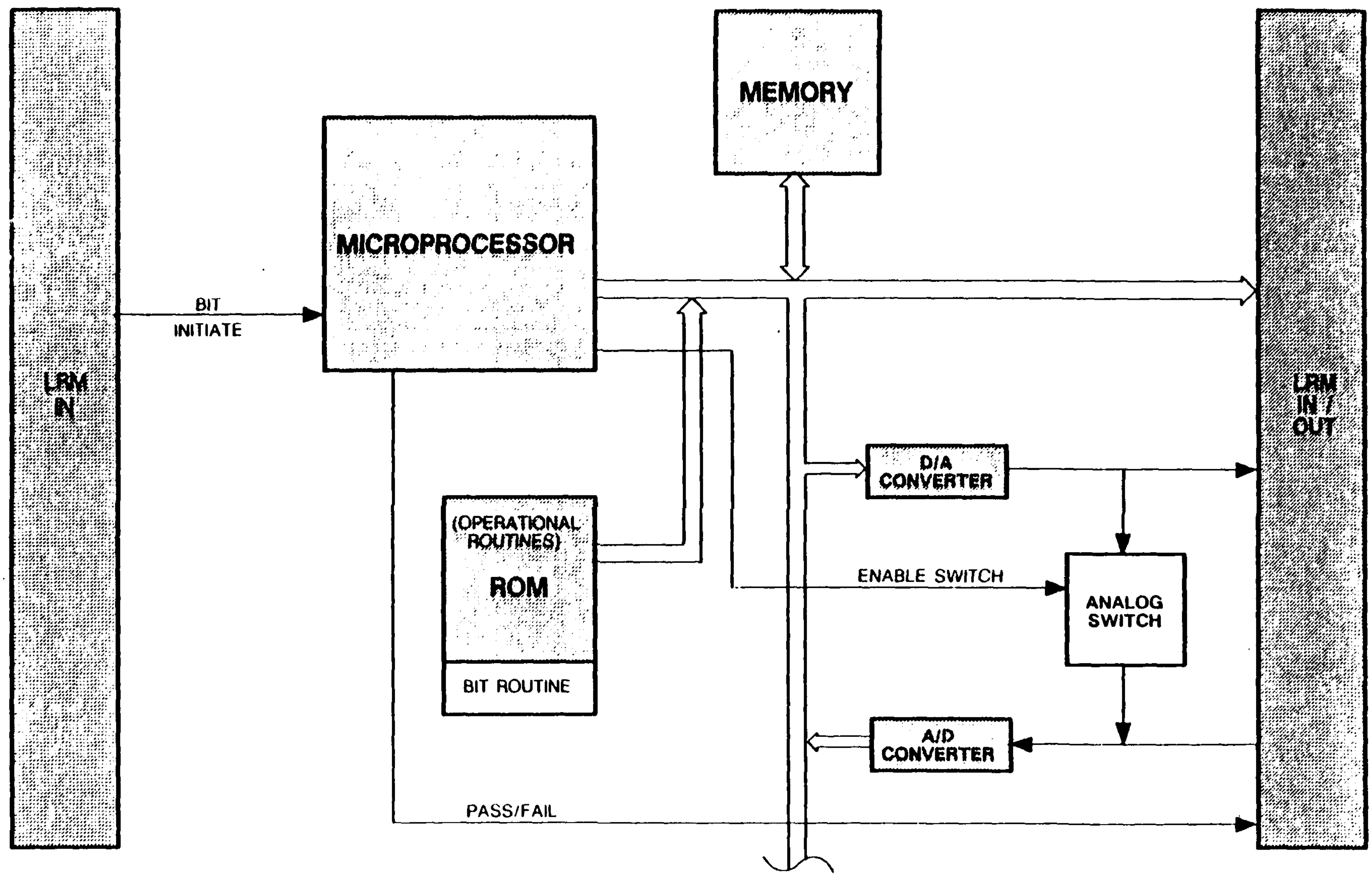


FIGURE 3 LEVEL II BLOCK DIAGRAM UTILIZING ANALOG WRAPAROUND

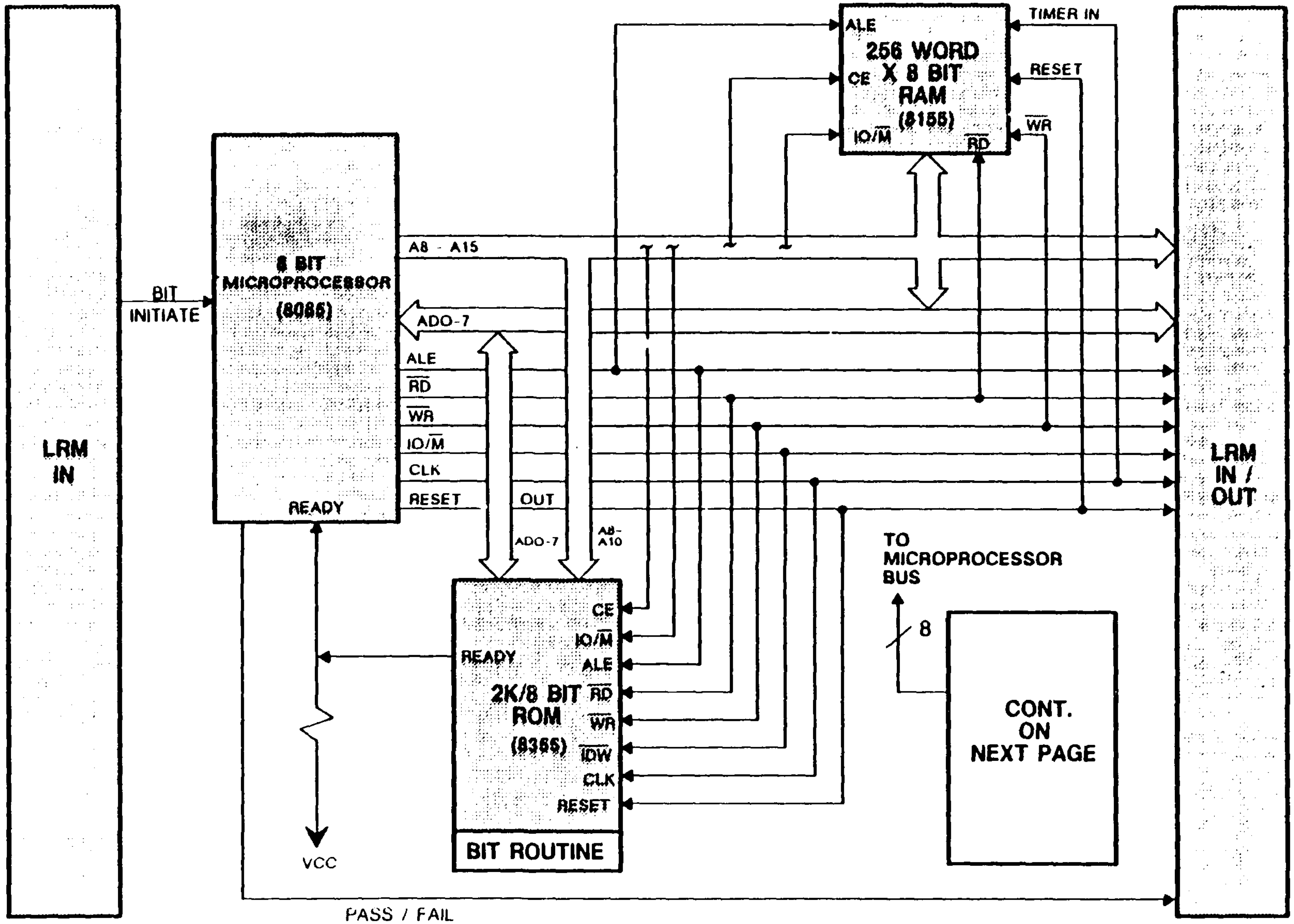


FIGURE 4 DEFAULT DESIGN - ANALOG WRAPAROUND

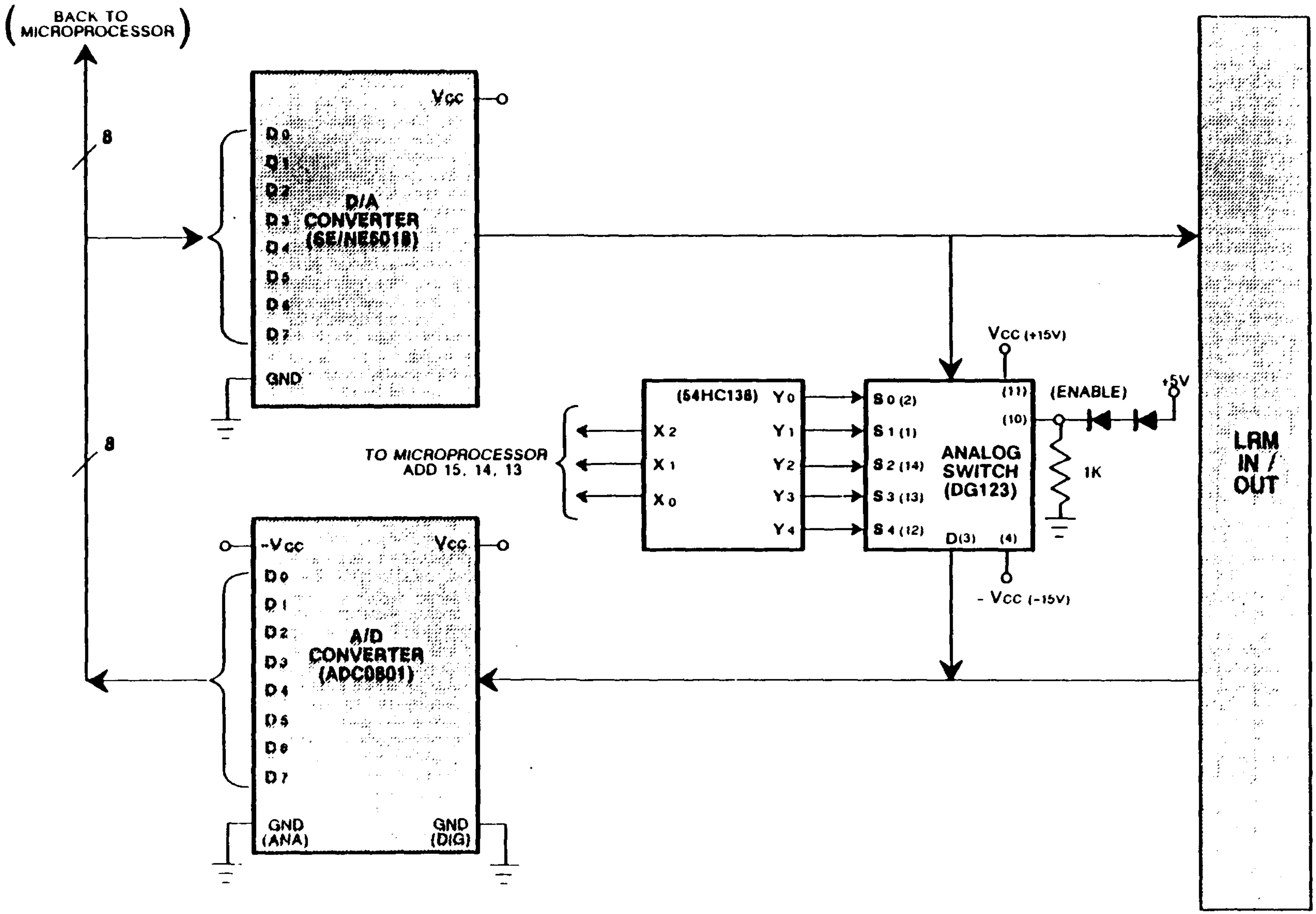


FIGURE 5 DEFAULT DESIGN – ANALOG WRAPAROUND

PAGE 8 of 10

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND

CATEGORY: LONG TUTORIAL

SUBCATEGORY: PARTS DATA TABLE

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☒ GRAPHIC ☐ EQUATIONS ☐

DATA:

NUMBER/NAME	AREA *(sq in)*	# OF PINS	POWER TYPICAL	POWER MAX. *(mW)*	WEIGHT *(gms)*
MM54HCT138 3 to 8 LINE DECODER	0.243	16	350	500	2.6
DG123 ANALOG 5-CHANNEL SWITCH	0.227	14	525	750	2.25

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND	
CATEGORY: LONG TUTORIAL	**PAGE** 10 **of** 10
SUBCATEGORY: BIBLIOGRAPHY	
DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐	

DATA:

NONE REQUIRED

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND

CATEGORY: USER REQUESTED DATA	PAGE 1 of 1

SUBCATEGORY:

DATA TYPE: TEXT ☐ LIST ☒ TABLE ☐ GRAPHIC ☐ EQUATIONS ☐

DATA:

QUESTIONS	VARIABLE ASSIGNMENT
1. How many analog outputs are to be wrapped around?	v1
2. How many test patterns are required?	v2
3. What is the test pattern application rate?	v3
4. What is the CUT initialization time?	v4

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND

CATEGORY: EQUATIONS	**PAGE** 1 **of** 2

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

I) VARIABLE DEFINITION

n1 = Number of 3 to 8 Line Decoders (MM54HCT138)

n2 = Number of Analog Switches (DG123)

v1 = Number of analog outputs to be wrapped around

v2 = Number of test patterns required

v3 = Test pattern application rate

v4 = CUT initialization time

II) COMPONENT DETERMINATION EQUATIONS

n1 = 1

n2 = v1/5

III) PENALTY EQUATIONS

a) AREA (sq in)

Area of BIT chips = (0.243)n1 + (0.227)n2

Total Area of BIT circuitry = (Total Area of chips)+15% for PC traces

= 1.15 (Area of BIT chips)

b) WEIGHT (gms)

Weight of BIT chips = (2.6)n1 + (2.25)n2

Weight of BIT circuitry= Weight of BIT chips + 10% for Weight of Solder

= 1.1 (Weight of chips)

LIBRARY ELEMENT DATA SHEET

BIT TECHNIQUE: ANALOG WRAPAROUND

CATEGORY: EQUATIONS | **PAGE** 2 **of** 2

SUBCATEGORY: (DATA NOT TO BE DISPLAYED)

DATA TYPE: TEXT ☐ LIST ☐ TABLE ☐ GRAPHIC ☐ EQUATIONS ☒

DATA:

III) PENALTY EQUATIONS (CONT)

c) POWER (mW)

Maximum Power of Bit Chips = (500)n1 + (750)n2

d) TEST TIME

Test Time = (v2)(v3) + v4

PARAGRAPH 7.0

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BIBLIOGRAPHY

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